EEL 4744

Menu

- A/D system on the XMEGA
- A/D Converter Example: EEG
- Analog-to-Digital Conversion
  - >Basic Charge-Redistribution A/D
- Analog-to-Digital Conversion
  - >What should the answers be?
  - >Example of 2-, 4-, … 8-bit conversions

See examples on web-site:
doc8331, doc8032, doc8385

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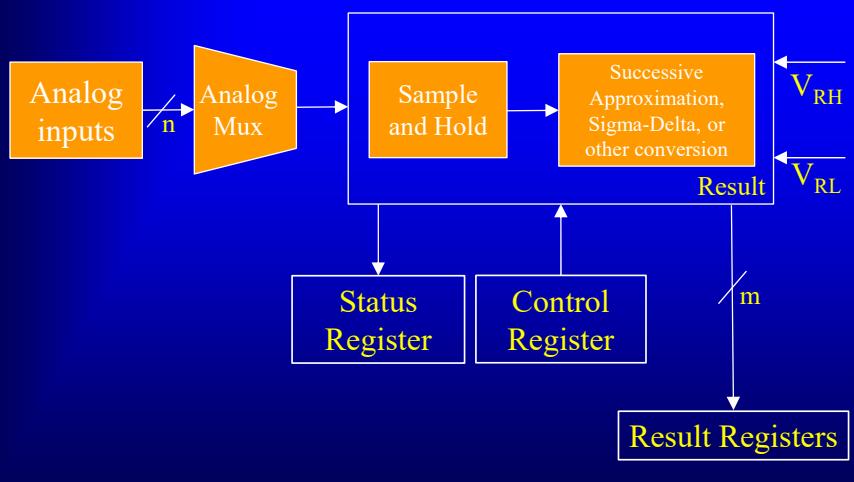
Analog-to-Digital Conversion Process



2

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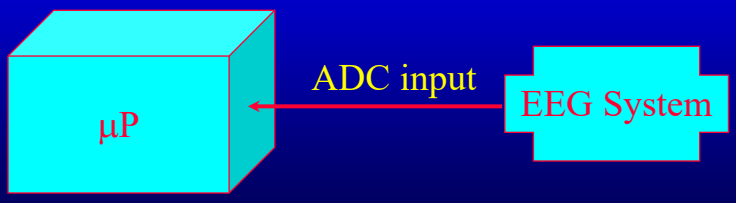
A/D EEG Example

- Problem Statement
  - Collect 100 samples of an EEG signal sampled at 125Hz
  - Place the 100 samples starting at location EEG
  - The EEG signal is amplified and is presented as a 0 – 5 V level analog signal to the A/D (after amplifying and filtering from between 0 and 50 μV, i.e., gain of 100,000)



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A/D EEG Example

- 5 V is too much for the XMEGA
  - > Use differential input and gain of ½ …
- f_S = 125 Hz, T_S = 1/125 = 0.008 s = 8 ms
  - > I.e., collect a sample every 8 ms
  - > Use a timer to generate an interrupt every 8 ms
- Pick any single-sided un-signed analog input (depending on gain stage)
- Single channel
- Single Scan
  - > You might want to assume noisy data, so instead of single scans, take 4 "quick" samples and then store the average
  - > "Quick" must mean **MUCH** quicker than the sampling rate, e.g., 0.08ms

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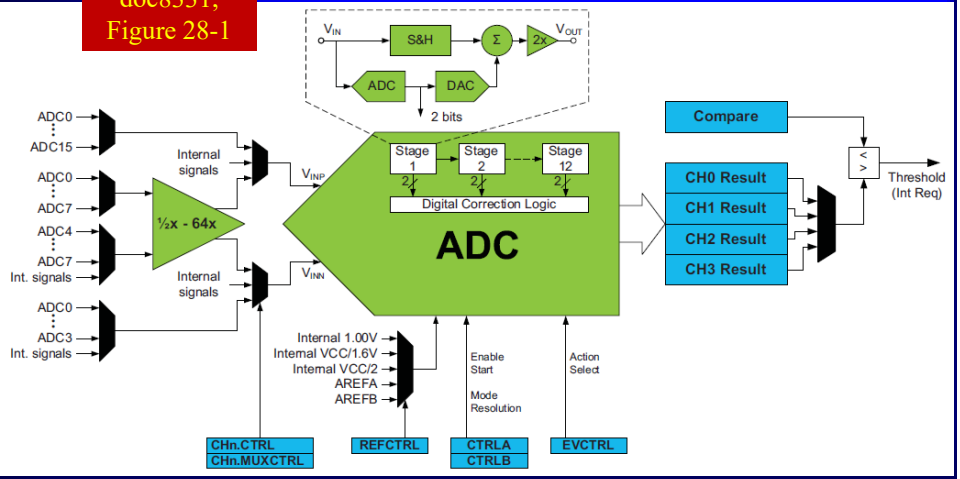
XMEGA ADC Block Diagram

doc8331, Figure 28-1



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XMEGA ADC Features

See doc8331, Section 28.1

- 12-bit resolution
- Up to 2Msamples/sec
  - > 2 inputs sampled simultaneously
  - > 4 inputs sampled within 1.5µs (667kHz)
- Differential or single-ended input
  - > Differential inputs with or without gain
    - Gains: ½ ×, 1×, 2×, 4×, 8×, 16×, 32x, 64×
- Single scan or continuous scans
- Signed or unsigned results
- Internal and external reference options
- Optional event triggered conversion
- Four conversion channels with individual input control and result register
  - > Enable four parallel configurations and results

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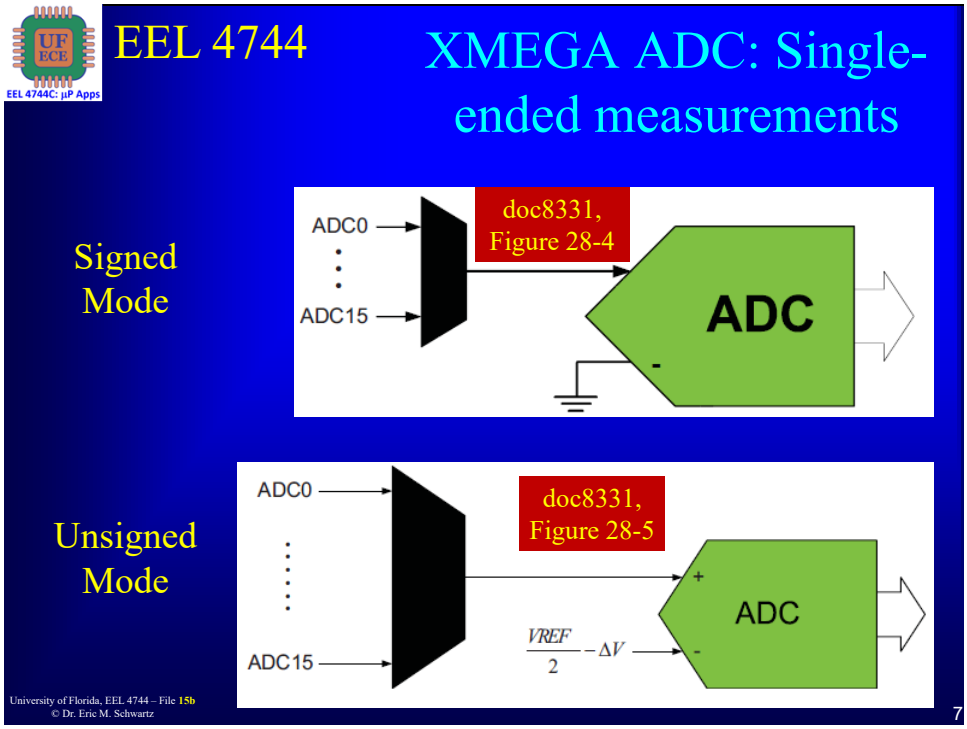
EEL 4744
XMEGA ADC: Single-ended measurements
Signed Mode
ADC0
ADC15
ADC
doc8331, Figure 28-4
Unsigned Mode
ADC0
ADC15
ADC
VREF/2 − ΔV
doc8331, Figure 28-5
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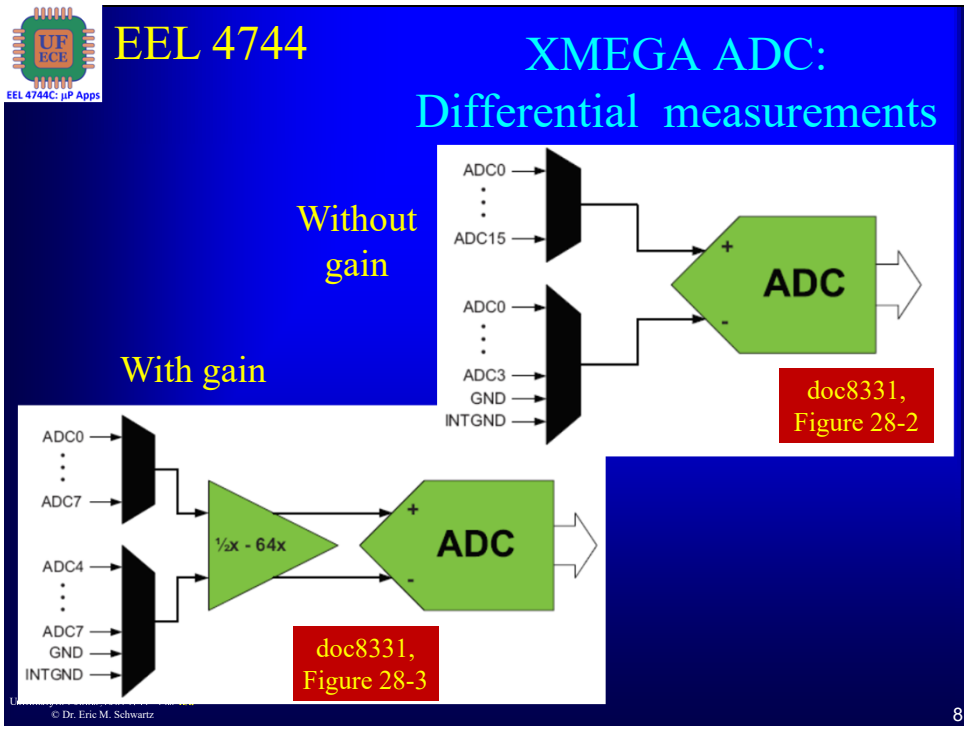
EEL 4744
XMEGA ADC: Differential measurements
Without gain
ADC0
ADC15
ADC0
ADC3
GND
INTGND
ADC
doc8331, Figure 28-2
With gain
ADC0
ADC7
ADC4
ADC7
GND
INTGND
½x - 64x
ADC
doc8331, Figure 28-3
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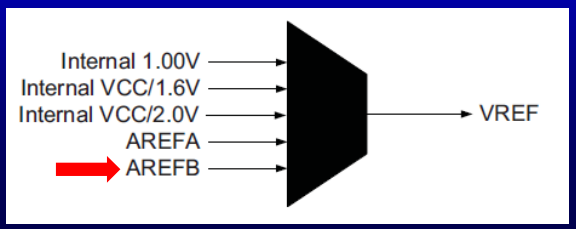
See doc8331, Section 28.5

XMEGA Voltage Reference

- Voltage reference (VREF) for the ADC is set to one of the following
  - >Internal 1.00V
  - >Internal Vcc/1.6V (=2.0625V for Vcc=3.3V)
  - >Internal Vcc/2V
  - >External voltage at AREF pin on PORTA
  - **>External voltage at AREF pin on PORTB (for µPAD)**
    - **– PB0 = V_{REF}**
    - **– PB1 = ADC GND**

doc8331, Figure 28-8



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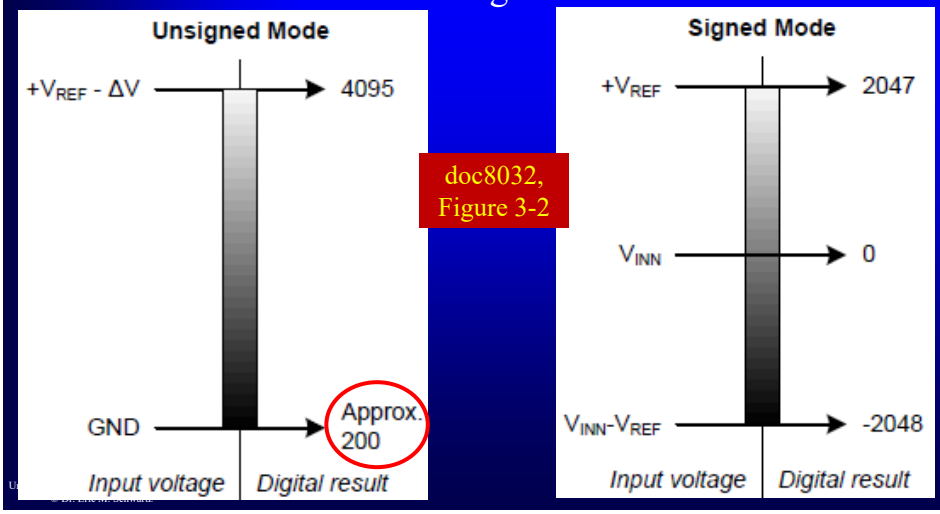
XMEGA Offset in Unsigned mode

- Note the offset in unsigned mode
  - >Used to detect zero-crossings

doc8032, Figure 3-2



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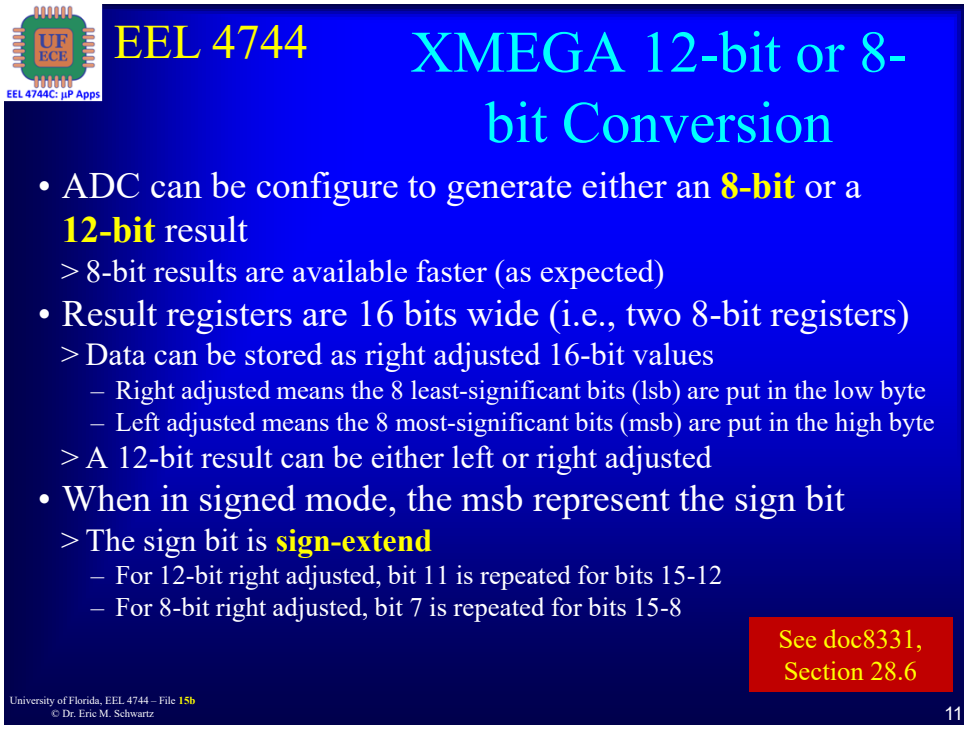
EEL 4744
XMEGA 12-bit or 8-bit Conversion
• ADC can be configure to generate either an 8-bit or a 12-bit result
> 8-bit results are available faster (as expected)
• Result registers are 16 bits wide (i.e., two 8-bit registers)
> Data can be stored as right adjusted 16-bit values
– Right adjusted means the 8 least-significant bits (lsb) are put in the low byte
– Left adjusted means the 8 most-significant bits (msb) are put in the high byte
> A 12-bit result can be either left or right adjusted
• When in signed mode, the msb represent the sign bit
> The sign bit is sign-extend
– For 12-bit right adjusted, bit 11 is repeated for bits 15-12
– For 8-bit right adjusted, bit 7 is repeated for bits 15-8
See doc8331, Section 28.6
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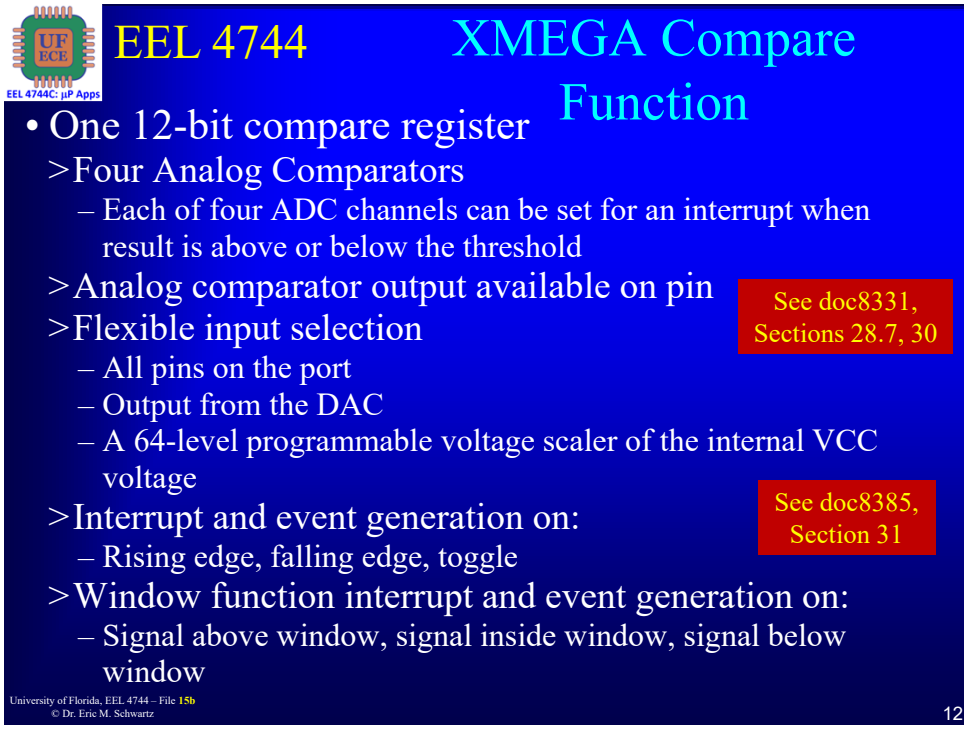
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XMEGA Compare Function
• One 12-bit compare register
> Four Analog Comparators
– Each of four ADC channels can be set for an interrupt when result is above or below the threshold
> Analog comparator output available on pin
> Flexible input selection
– All pins on the port
– Output from the DAC
– A 64-level programmable voltage scaler of the internal VCC voltage
See doc8331, Sections 28.7, 30
> Interrupt and event generation on:
– Rising edge, falling edge, toggle
See doc8385, Section 31
> Window function interrupt and event generation on:
– Signal above window, signal inside window, signal below window
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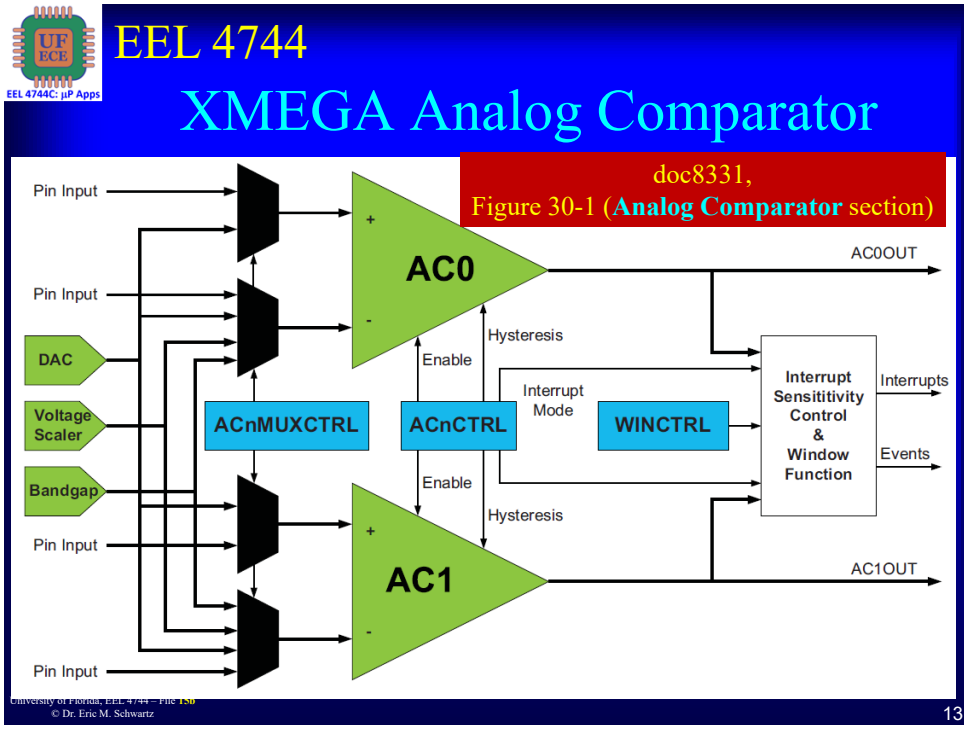
EEL 4744
XMEGA Analog Comparator
doc8331,
Figure 30-1 (Analog Comparator section)
Pin Input
Pin Input
DAC
Voltage Scaler
Bandgap
Pin Input
Pin Input
AC0
AC1
ACnMUXCTRL
ACnCTRL
WINCTRL
Enable
Hysteresis
Interrupt Mode
Enable
Hysteresis
AC0OUT
AC1OUT
Interrupt Sensitivity Control & Window Function
Interrupts
Events
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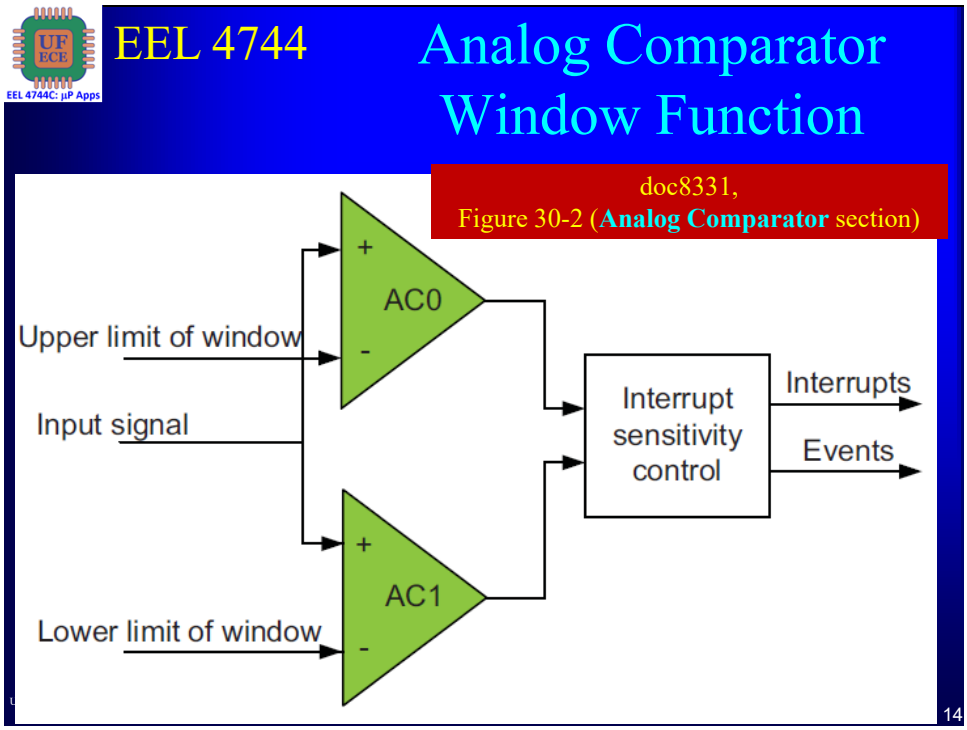
EEL 4744
Analog Comparator Window Function
doc8331,
Figure 30-2 (Analog Comparator section)
Upper limit of window
Input signal
Lower limit of window
AC0
AC1
Interrupt sensitivity control
Interrupts
Events
14

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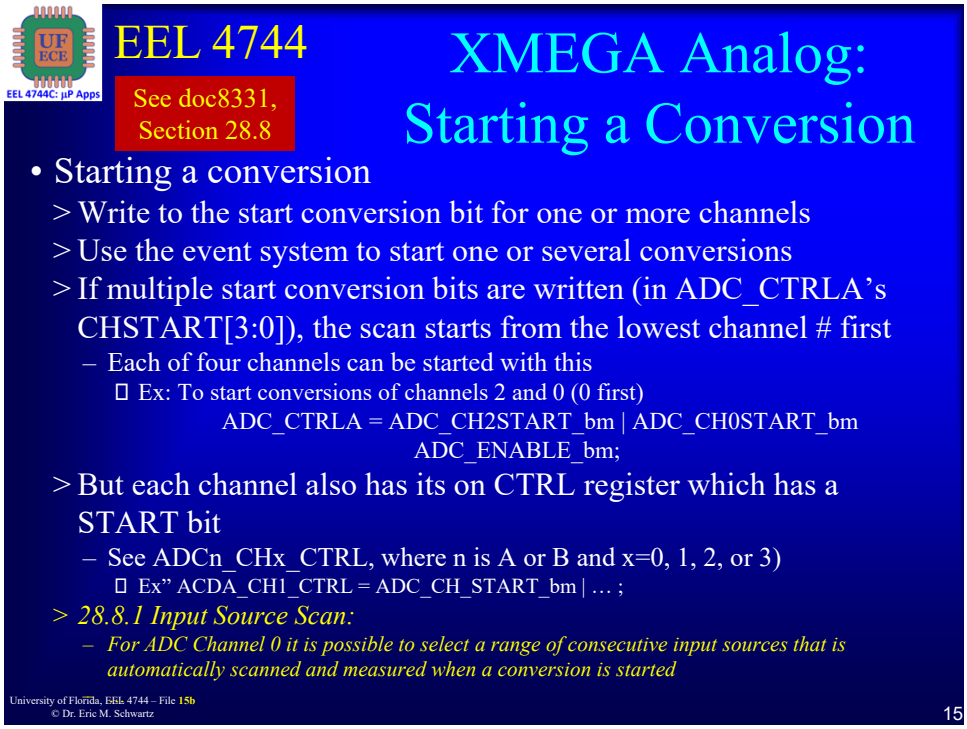
EEL 4744
See doc8331, Section 28.8
XMEGA Analog: Starting a Conversion
• Starting a conversion
> Write to the start conversion bit for one or more channels
> Use the event system to start one or several conversions
> If multiple start conversion bits are written (in ADC_CTRLA's CHSTART[3:0]), the scan starts from the lowest channel # first
– Each of four channels can be started with this
Ex: To start conversions of channels 2 and 0 (0 first)
ADC_CTRLA = ADC_CH2START_bm | ADC_CH0START_bm
ADC_ENABLE_bm;
> But each channel also has its on CTRL register which has a START bit
– See ADCn_CHx_CTRL, where n is A or B and x=0, 1, 2, or 3)
Ex" ACDA_CH1_CTRL = ADC_CH_START_bm | … ;
> 28.8.1 Input Source Scan:
– For ADC Channel 0 it is possible to select a range of consecutive input sources that is automatically scanned and measured when a conversion is started
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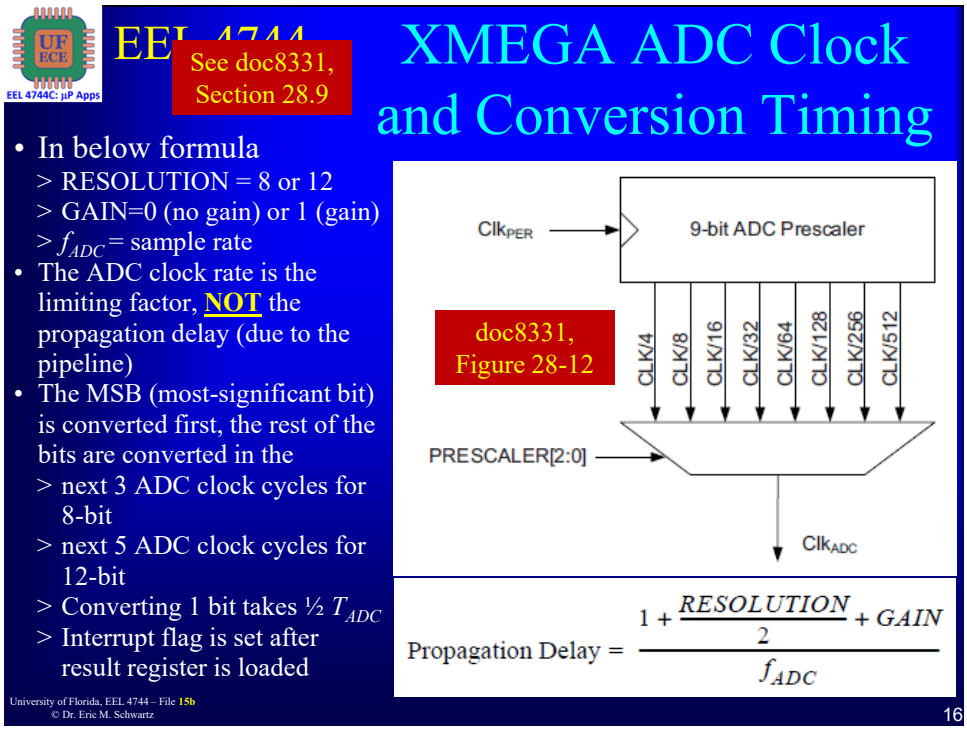
EEL 4744
See doc8331, Section 28.9
XMEGA ADC Clock and Conversion Timing
• In below formula
> RESOLUTION = 8 or 12
> GAIN=0 (no gain) or 1 (gain)
> f_{ADC} = sample rate
• The ADC clock rate is the limiting factor, NOT the propagation delay (due to the pipeline)
• The MSB (most-significant bit) is converted first, the rest of the bits are converted in the
> next 3 ADC clock cycles for 8-bit
> next 5 ADC clock cycles for 12-bit
> Converting 1 bit takes ½ T_{ADC}
> Interrupt flag is set after result register is loaded
doc8331, Figure 28-12
ClkPER
9-bit ADC Prescaler
CLK/4
CLK/8
CLK/16
CLK/32
CLK/64
CLK/128
CLK/256
CLK/512
PRESCALER[2:0]
ClkADC
Propagation Delay = $\frac{1 + \frac{RESOLUTION}{2} + GAIN}{f_{ADC}}$
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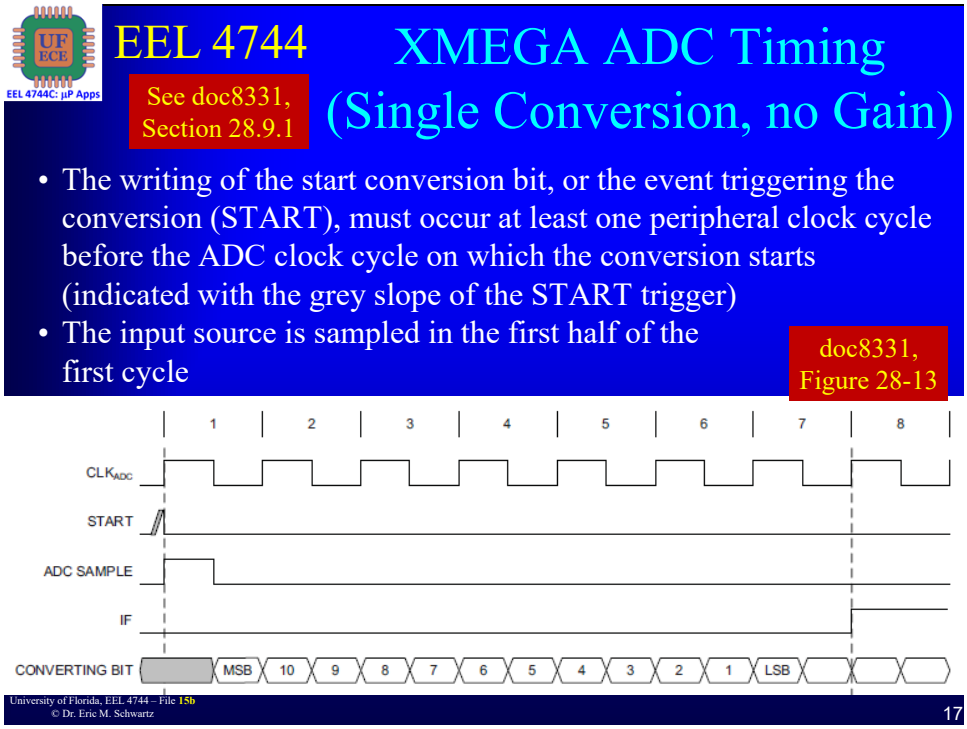
EEL 4744
See doc8331, Section 28.9.1
XMEGA ADC Timing (Single Conversion, no Gain)
• The writing of the start conversion bit, or the event triggering the conversion (START), must occur at least one peripheral clock cycle before the ADC clock cycle on which the conversion starts (indicated with the grey slope of the START trigger)
• The input source is sampled in the first half of the first cycle
doc8331, Figure 28-13
1 2 3 4 5 6 7 8
CLKADC
START
ADC SAMPLE
IF
CONVERTING BIT
MSB 10 9 8 7 6 5 4 3 2 1 LSB
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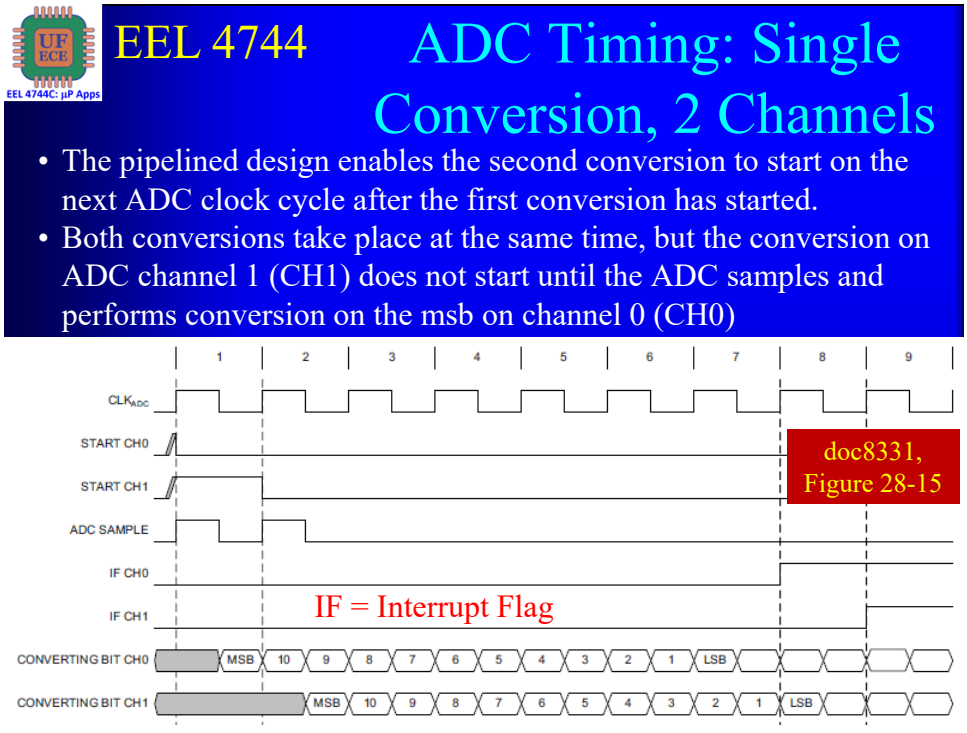
EEL 4744
ADC Timing: Single Conversion, 2 Channels
• The pipelined design enables the second conversion to start on the next ADC clock cycle after the first conversion has started.
• Both conversions take place at the same time, but the conversion on ADC channel 1 (CH1) does not start until the ADC samples and performs conversion on the msb on channel 0 (CH0)
1 2 3 4 5 6 7 8 9
CLKADC
START CH0
START CH1
ADC SAMPLE
IF CH0
IF CH1
IF = Interrupt Flag
CONVERTING BIT CH0
MSB 10 9 8 7 6 5 4 3 2 1 LSB
CONVERTING BIT CH1
MSB 10 9 8 7 6 5 4 3 2 1 LSB
doc8331, Figure 28-15

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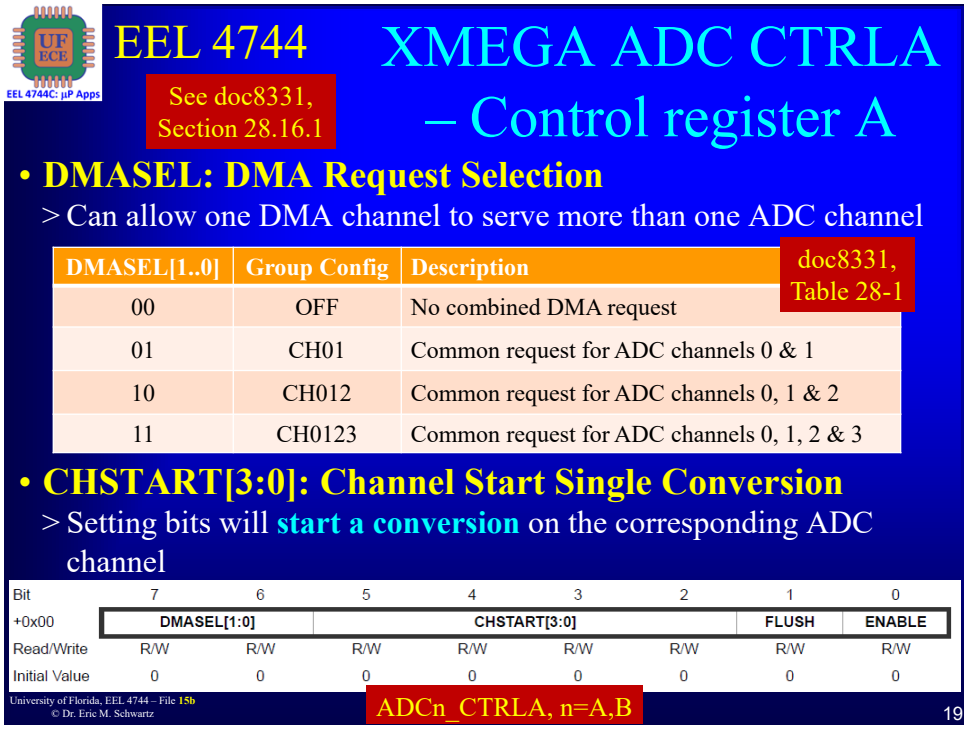
EEL 4744
See doc8331, Section 28.16.1
XMEGA ADC CTRLA – Control register A
• DMASEL: DMA Request Selection
> Can allow one DMA channel to serve more than one ADC channel
DMASEL[1..0] | Group Config | Description
00 | OFF | No combined DMA request
01 | CH01 | Common request for ADC channels 0 & 1
10 | CH012 | Common request for ADC channels 0, 1 & 2
11 | CH0123 | Common request for ADC channels 0, 1, 2 & 3
doc8331, Table 28-1
• CHSTART[3:0]: Channel Start Single Conversion
> Setting bits will start a conversion on the corresponding ADC channel
Bit 7 6 5 4 3 2 1 0
+0x00 DMASEL[1:0] CHSTART[3:0] FLUSH ENABLE
Read/Write R/W R/W R/W R/W R/W R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
ADCn_CTRLA, n=A,B
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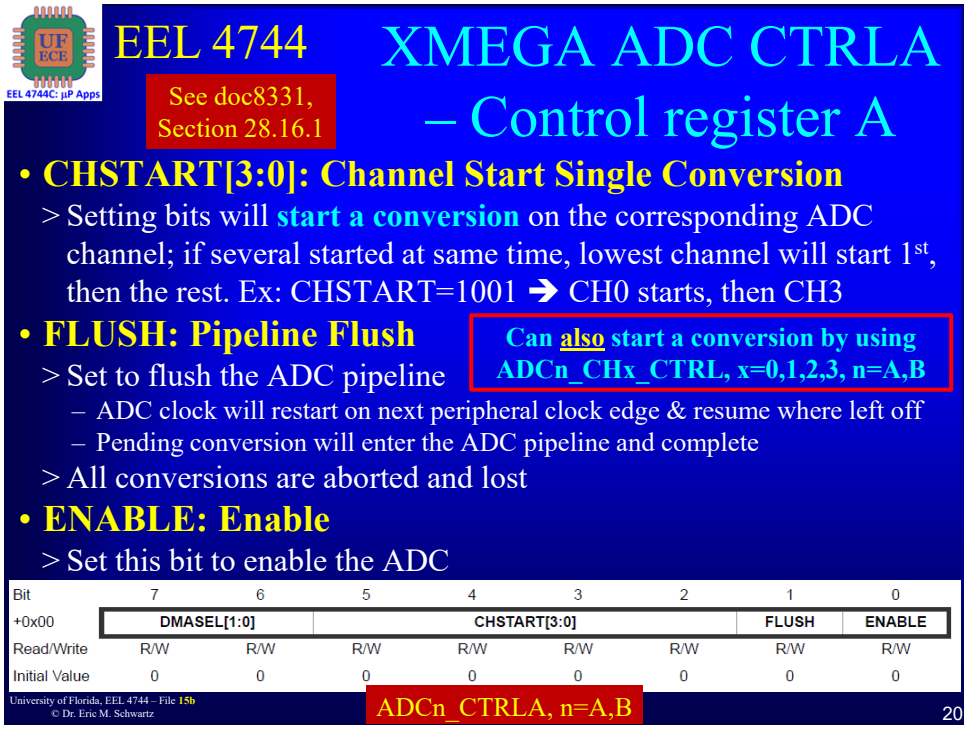
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See doc8331, Section 28.16.1
XMEGA ADC CTRLA – Control register A
• CHSTART[3:0]: Channel Start Single Conversion
> Setting bits will start a conversion on the corresponding ADC channel; if several started at same time, lowest channel will start 1st, then the rest. Ex: CHSTART=1001 ➔ CH0 starts, then CH3
• FLUSH: Pipeline Flush
> Set to flush the ADC pipeline
– ADC clock will restart on next peripheral clock edge & resume where left off
– Pending conversion will enter the ADC pipeline and complete
> All conversions are aborted and lost
Can also start a conversion by using ADCn_CHx_CTRL, x=0,1,2,3, n=A,B
• ENABLE: Enable
> Set this bit to enable the ADC
Bit 7 6 5 4 3 2 1 0
+0x00 DMASEL[1:0] CHSTART[3:0] FLUSH ENABLE
Read/Write R/W R/W R/W R/W R/W R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
ADCn_CTRLA, n=A,B
20

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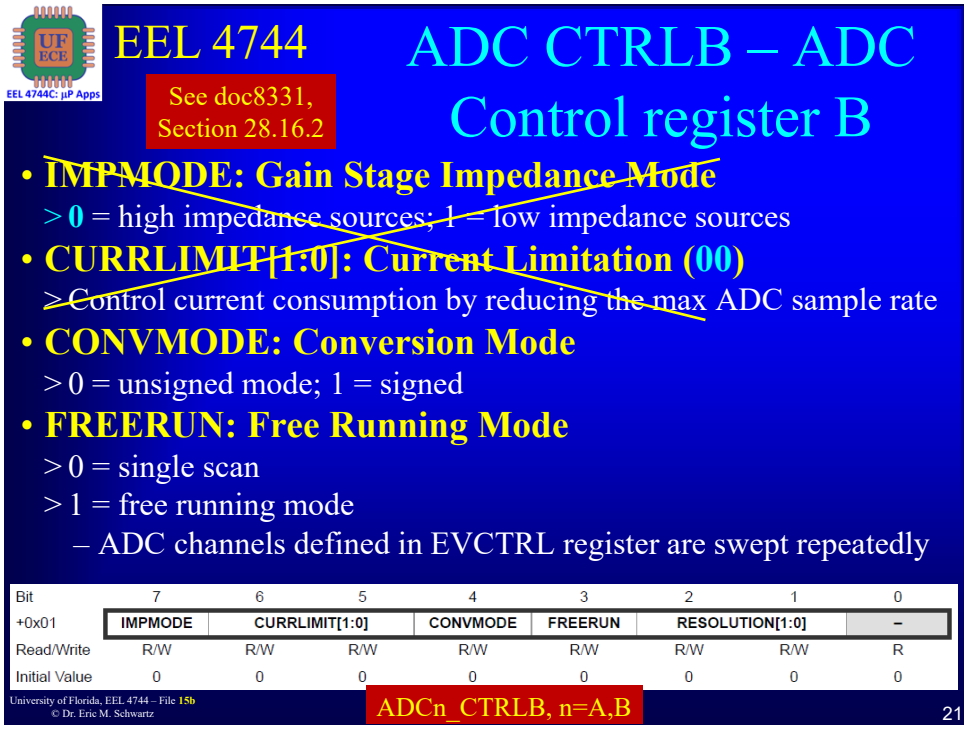
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ADC CTRLB – ADC Control register B
See doc8331, Section 28.16.2
• IMPMODE: Gain Stage Impedance Mode
> 0 = high impedance sources; 1 = low impedance sources
• CURRLIMIT[1:0]: Current Limitation (00)
> Control current consumption by reducing the max ADC sample rate
• CONVMODE: Conversion Mode
> 0 = unsigned mode; 1 = signed
• FREERUN: Free Running Mode
> 0 = single scan
> 1 = free running mode
– ADC channels defined in EVCTRL register are swept repeatedly
Bit 7 6 5 4 3 2 1 0
+0x01 IMPMODE CURRLIMIT[1:0] CONVMODE FREERUN RESOLUTION[1:0] –
Read/Write R/W R/W R/W R/W R/W R/W R/W R
Initial Value 0 0 0 0 0 0 0 0
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ADCn_CTRLB, n=A,B
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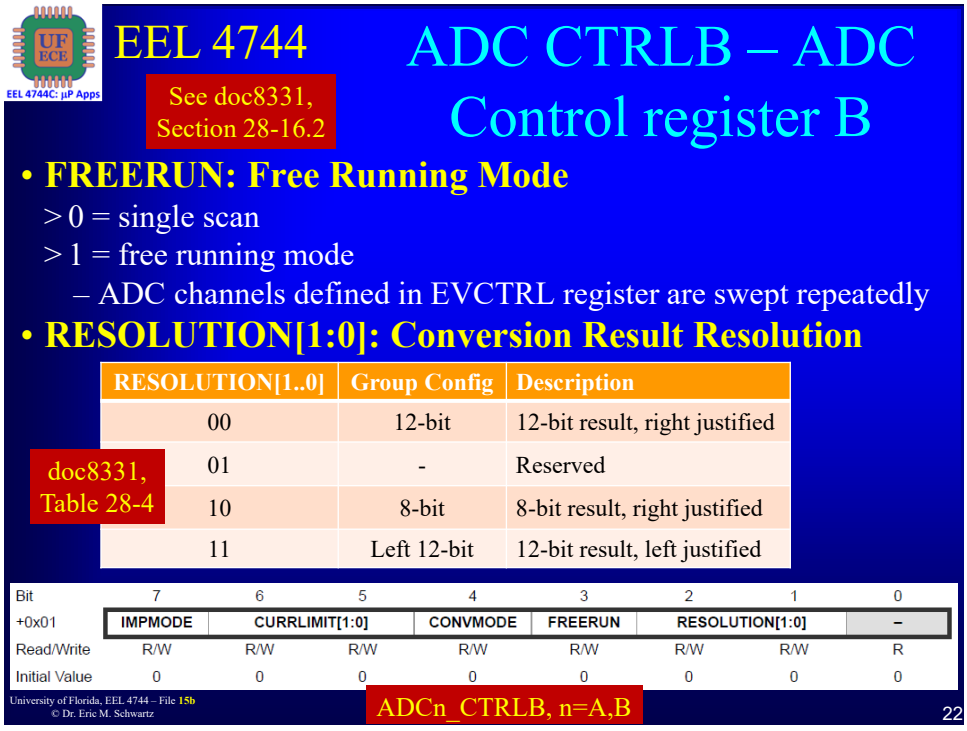
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ADC CTRLB – ADC Control register B
See doc8331, Section 28-16.2
• FREERUN: Free Running Mode
> 0 = single scan
> 1 = free running mode
– ADC channels defined in EVCTRL register are swept repeatedly
• RESOLUTION[1:0]: Conversion Result Resolution
RESOLUTION[1..0] Group Config Description
00 12-bit 12-bit result, right justified
01 - Reserved
10 8-bit 8-bit result, right justified
11 Left 12-bit 12-bit result, left justified
doc8331, Table 28-4
Bit 7 6 5 4 3 2 1 0
+0x01 IMPMODE CURRLIMIT[1:0] CONVMODE FREERUN RESOLUTION[1:0] –
Read/Write R/W R/W R/W R/W R/W R/W R/W R
Initial Value 0 0 0 0 0 0 0 0
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ADCn_CTRLB, n=A,B
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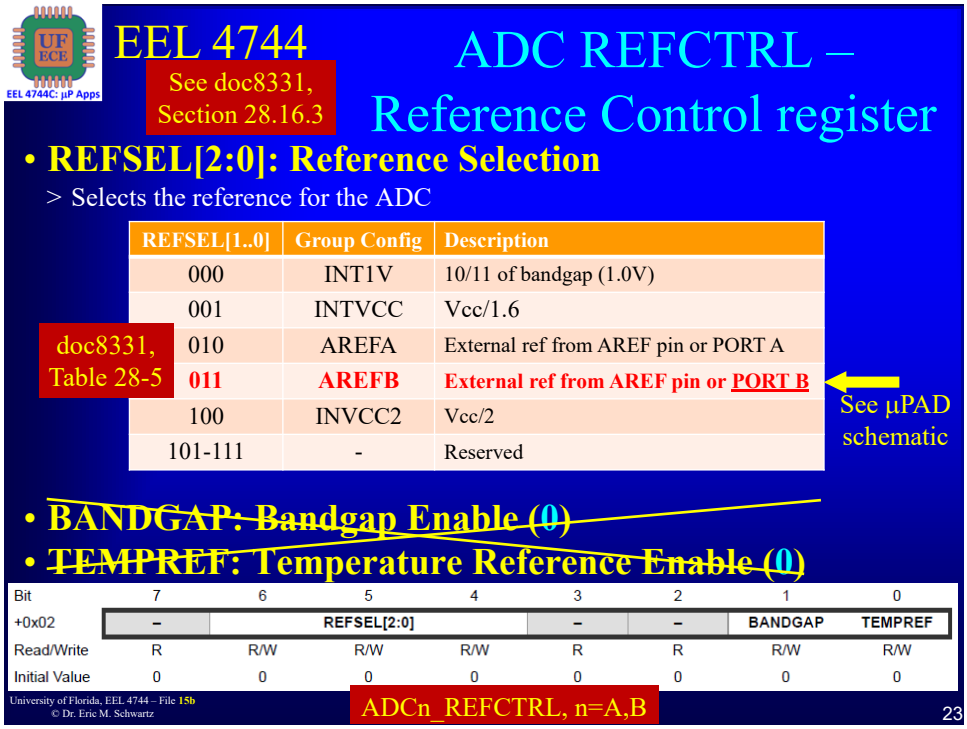
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See doc8331, Section 28.16.3
ADC REFCTRL – Reference Control register
• REFSEL[2:0]: Reference Selection
> Selects the reference for the ADC
REFSEL[1..0] | Group Config | Description
000 | INT1V | 10/11 of bandgap (1.0V)
001 | INTVCC | Vcc/1.6
010 | AREFA | External ref from AREF pin or PORT A
011 | AREFB | External ref from AREF pin or PORT B
100 | INVCC2 | Vcc/2
101-111 | - | Reserved
doc8331, Table 28-5
See µPAD schematic
• BANDGAP: Bandgap Enable (0)
• TEMPREF: Temperature Reference Enable (0)
Bit 7 6 5 4 3 2 1 0
+0x02 – REFSEL[2:0] – – BANDGAP TEMPREF
Read/Write R R/W R/W R/W R R R/W R/W
Initial Value 0 0 0 0 0 0 0 0
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ADCn_REFCTRL, n=A,B
23

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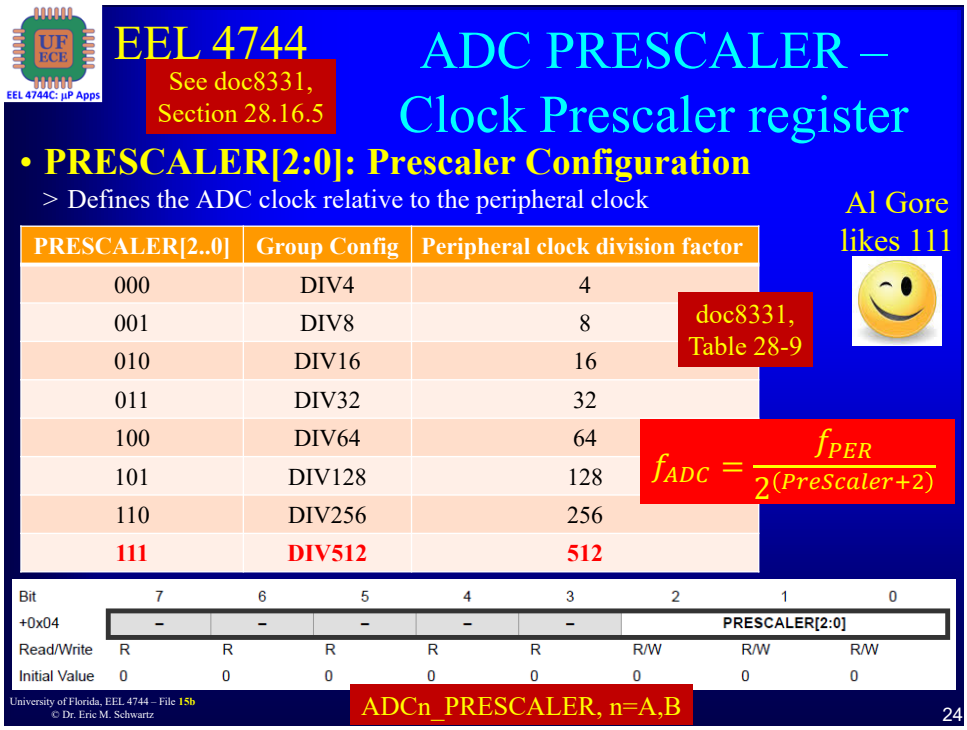
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See doc8331, Section 28.16.5
ADC PRESCALER – Clock Prescaler register
• PRESCALER[2:0]: Prescaler Configuration
> Defines the ADC clock relative to the peripheral clock
Al Gore likes 111
PRESCALER[2..0] | Group Config | Peripheral clock division factor
000 | DIV4 | 4
001 | DIV8 | 8
010 | DIV16 | 16
011 | DIV32 | 32
100 | DIV64 | 64
101 | DIV128 | 128
110 | DIV256 | 256
111 | DIV512 | 512
doc8331, Table 28-9
$f_{ADC} = \frac{f_{PER}}{2^{(PreScaler+2)}}$
Bit 7 6 5 4 3 2 1 0
+0x04 – – – – – PRESCALER[2:0]
Read/Write R R R R R R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
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ADCn_PRESCALER, n=A,B
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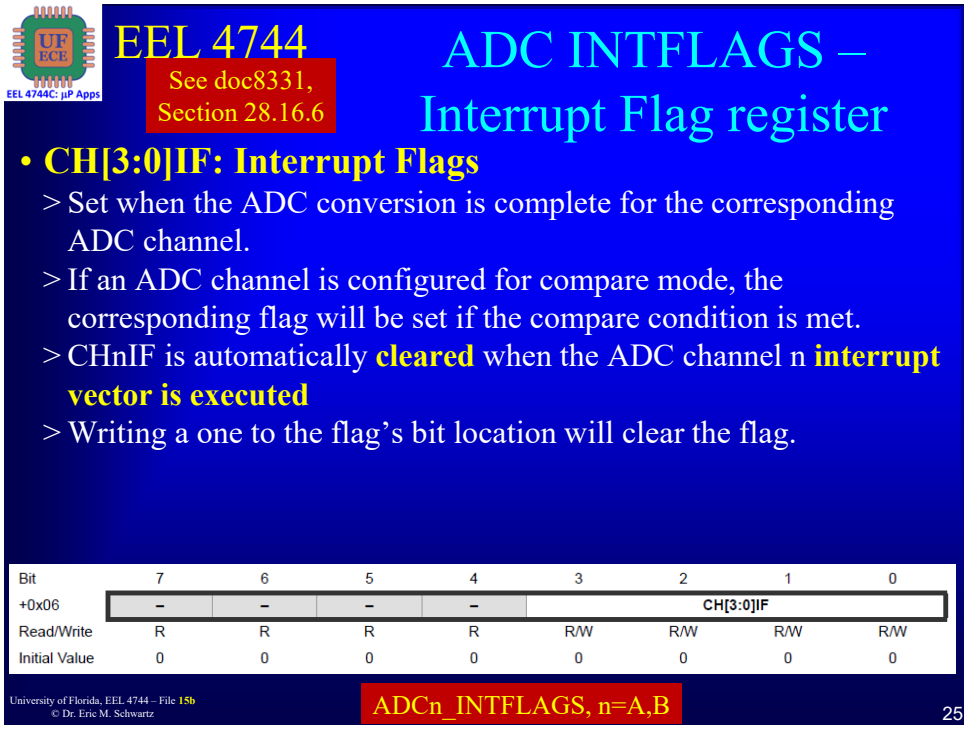
EEL 4744
See doc8331, Section 28.16.6
ADC INTFLAGS – Interrupt Flag register
• CH[3:0]IF: Interrupt Flags
> Set when the ADC conversion is complete for the corresponding ADC channel.
> If an ADC channel is configured for compare mode, the corresponding flag will be set if the compare condition is met.
> CHnIF is automatically cleared when the ADC channel n interrupt vector is executed
> Writing a one to the flag's bit location will clear the flag.
Bit 7 6 5 4 3 2 1 0
+0x06 – – – – CH[3:0]IF
Read/Write R R R R R/W R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
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ADCn_INTFLAGS, n=A,B
25

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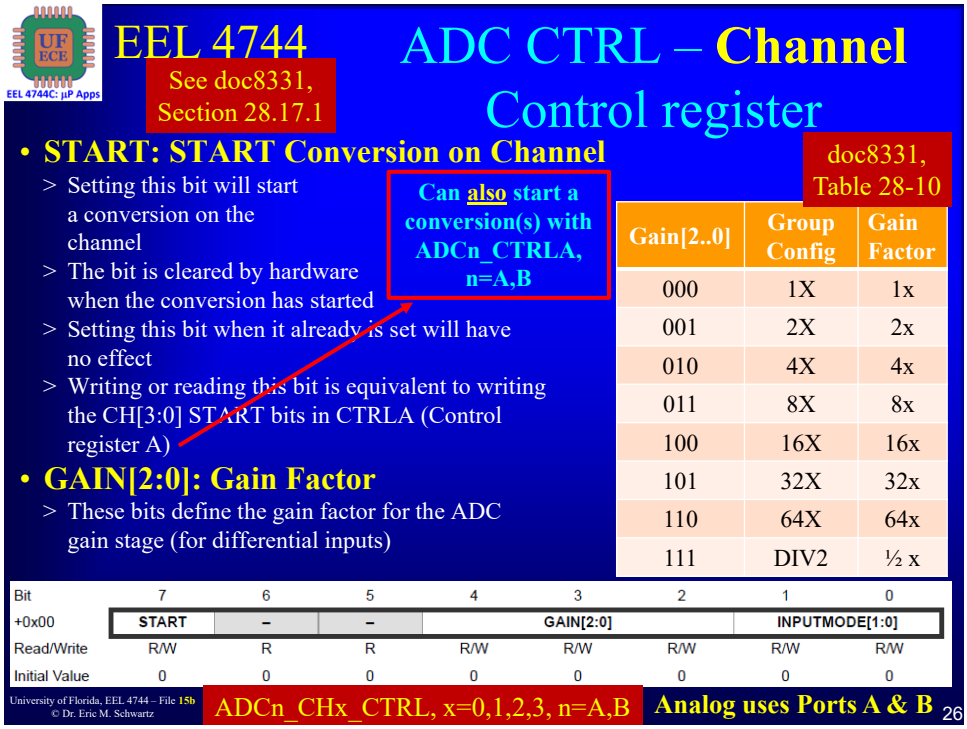
EEL 4744
See doc8331, Section 28.17.1
ADC CTRL – Channel Control register
• START: START Conversion on Channel
> Setting this bit will start a conversion on the channel
> The bit is cleared by hardware when the conversion has started
> Setting this bit when it already is set will have no effect
> Writing or reading this bit is equivalent to writing the CH[3:0] START bits in CTRLA (Control register A)
Can also start a conversion(s) with ADCn_CTRLA, n=A,B
• GAIN[2:0]: Gain Factor
> These bits define the gain factor for the ADC gain stage (for differential inputs)
doc8331, Table 28-10
Gain[2..0] | Group Config | Gain Factor
000 | 1X | 1x
001 | 2X | 2x
010 | 4X | 4x
011 | 8X | 8x
100 | 16X | 16x
101 | 32X | 32x
110 | 64X | 64x
111 | DIV2 | ½ x
Bit 7 6 5 4 3 2 1 0
+0x00 START – – GAIN[2:0] INPUTMODE[1:0]
Read/Write R/W R R R/W R/W R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
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ADCn_CHx_CTRL, x=0,1,2,3, n=A,B
Analog uses Ports A & B
26

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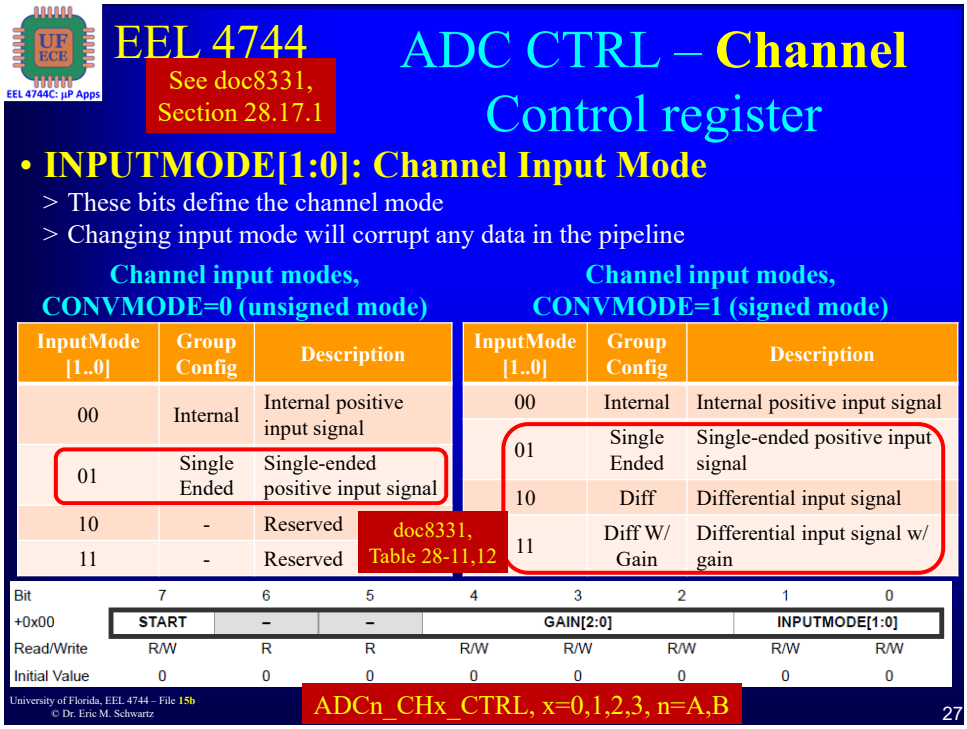
EEL 4744
See doc8331, Section 28.17.1
ADC CTRL – Channel Control register
• INPUTMODE[1:0]: Channel Input Mode
> These bits define the channel mode
> Changing input mode will corrupt any data in the pipeline
Channel input modes, CONVMODE=0 (unsigned mode)
InputMode [1..0] | Group Config | Description
00 | Internal | Internal positive input signal
01 | Single Ended | Single-ended positive input signal
10 | - | Reserved
11 | - | Reserved
Channel input modes, CONVMODE=1 (signed mode)
InputMode [1..0] | Group Config | Description
00 | Internal | Internal positive input signal
01 | Single Ended | Single-ended positive input signal
10 | Diff | Differential input signal
11 | Diff W/ Gain | Differential input signal w/ gain
doc8331, Table 28-11,12
Bit 7 6 5 4 3 2 1 0
+0x00 START – – GAIN[2:0] INPUTMODE[1:0]
Read/Write R/W R R R/W R/W R/W R/W R/W
Initial Value 0 0 0 0 0 0 0 0
ADCn_CHx_CTRL, x=0,1,2,3, n=A,B
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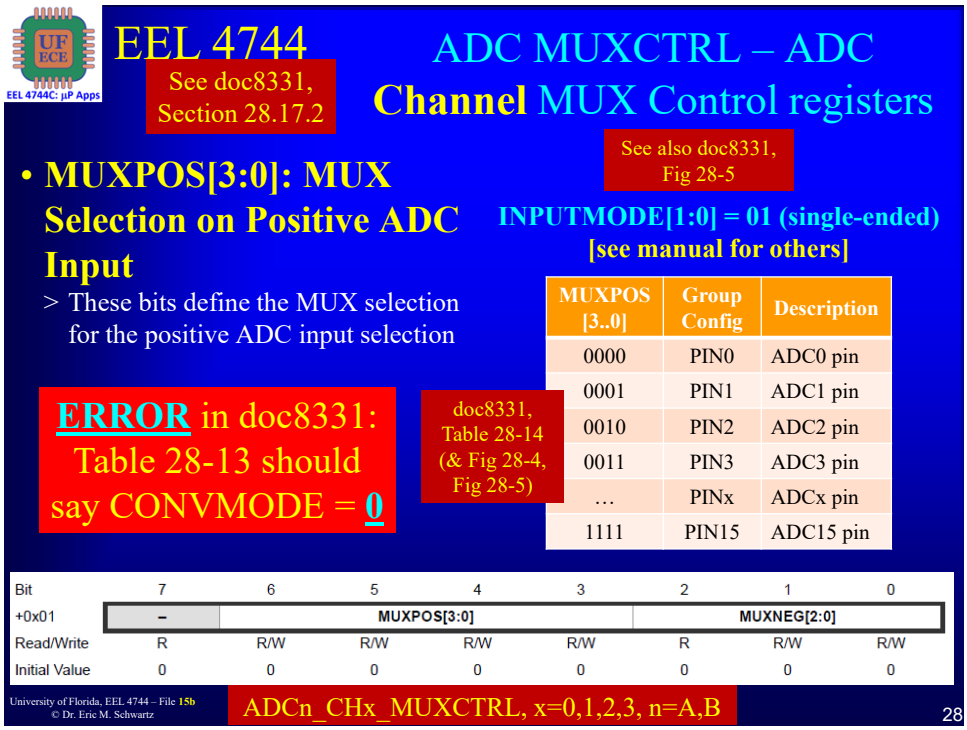
EEL 4744
See doc8331, Section 28.17.2
ADC MUXCTRL – ADC Channel MUX Control registers
See also doc8331, Fig 28-5
• MUXPOS[3:0]: MUX Selection on Positive ADC Input
> These bits define the MUX selection for the positive ADC input selection
INPUTMODE[1:0] = 01 (single-ended) [see manual for others]
MUXPOS [3..0] | Group Config | Description
0000 | PIN0 | ADC0 pin
0001 | PIN1 | ADC1 pin
0010 | PIN2 | ADC2 pin
0011 | PIN3 | ADC3 pin
… | PINx | ADCx pin
1111 | PIN15 | ADC15 pin
ERROR in doc8331: Table 28-13 should say CONVMODE = 0
doc8331, Table 28-14 (& Fig 28-4, Fig 28-5)
Bit 7 6 5 4 3 2 1 0
+0x01 – MUXPOS[3:0] MUXNEG[2:0]
Read/Write R R/W R/W R/W R/W R R/W R/W
Initial Value 0 0 0 0 0 0 0 0
ADCn_CHx_MUXCTRL, x=0,1,2,3, n=A,B
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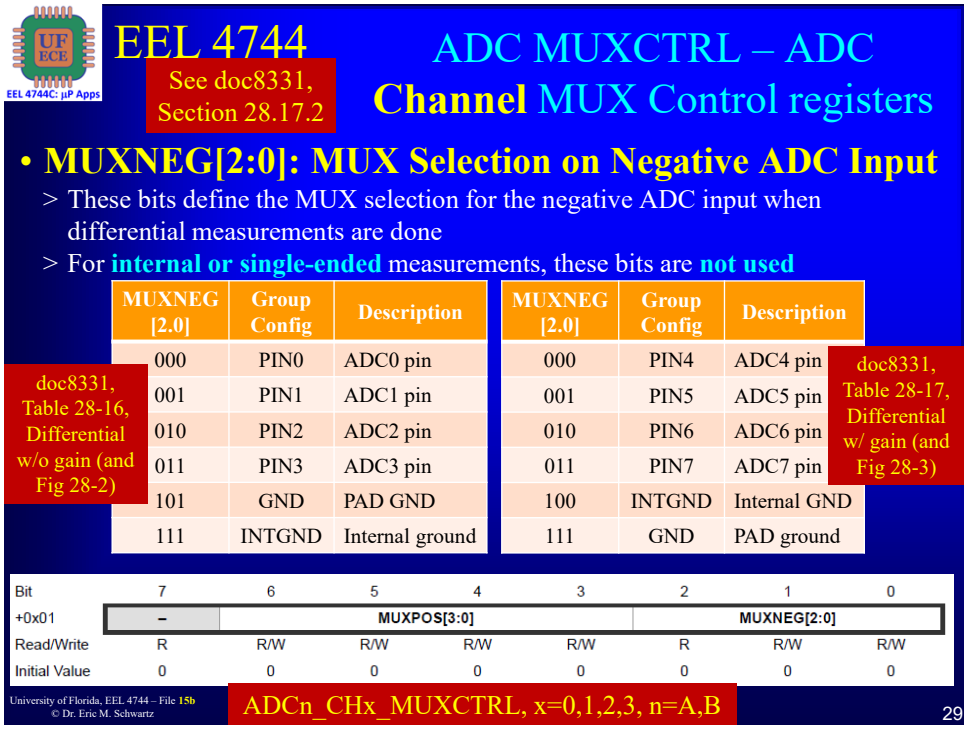

MUXNEG [2.0]	Group Config	Description
000	PIN0	ADC0 pin
001	PIN1	ADC1 pin
010	PIN2	ADC2 pin
011	PIN3	ADC3 pin
101	GND	PAD GND
111	INTGND	Internal ground

MUXNEG [2.0]	Group Config	Description
000	PIN4	ADC4 pin
001	PIN5	ADC5 pin
010	PIN6	ADC6 pin
011	PIN7	ADC7 pin
100	INTGND	Internal GND
111	GND	PAD ground

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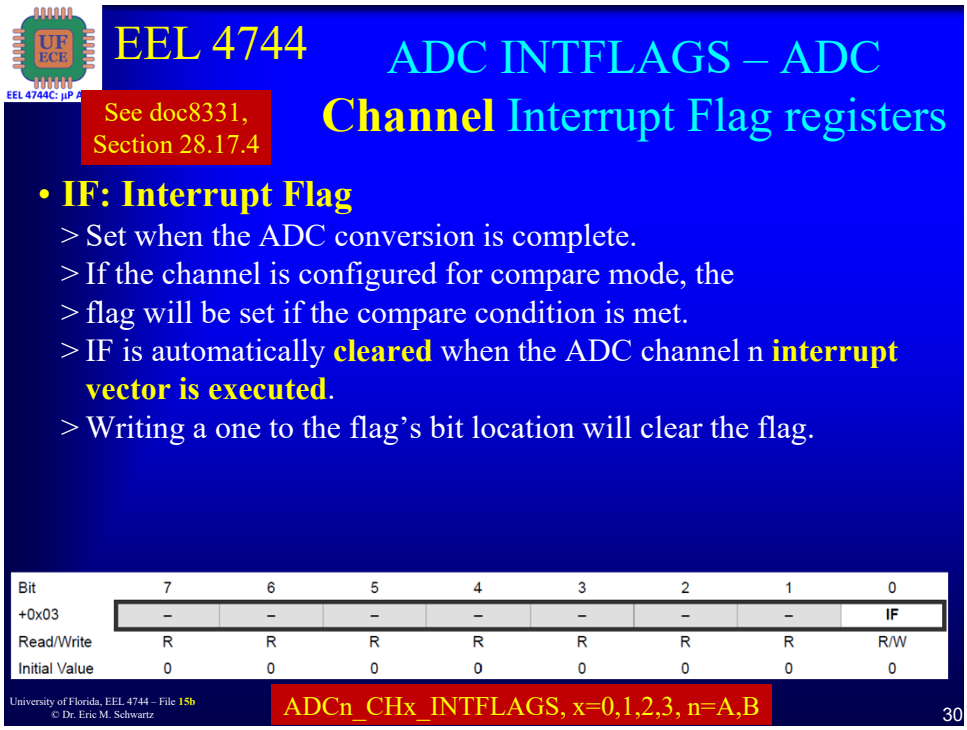

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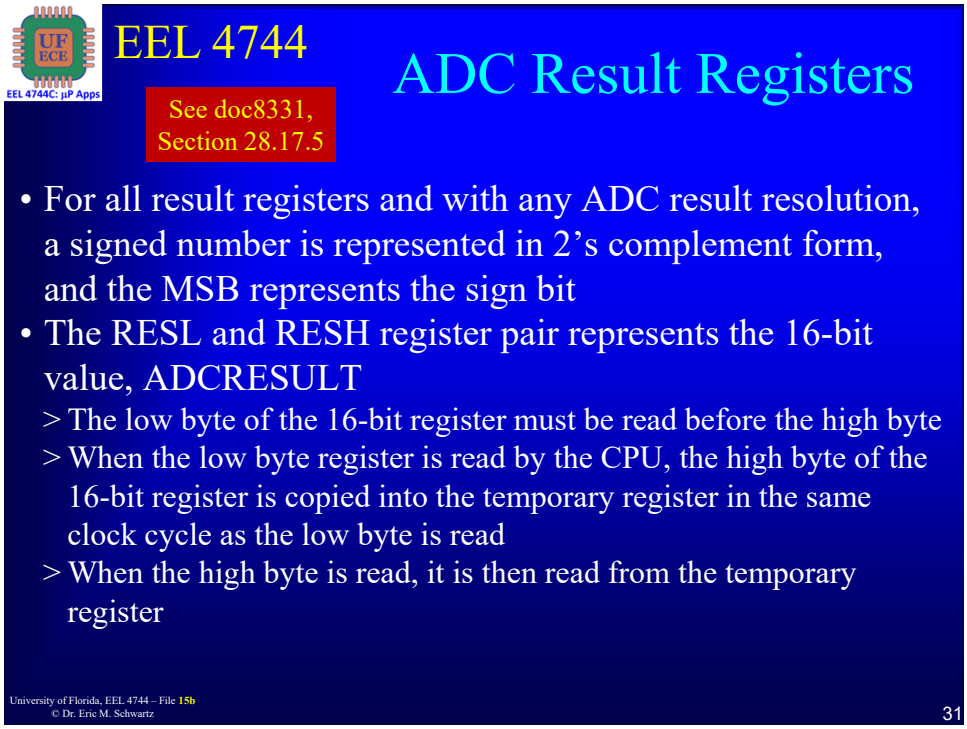
EEL 4744
See doc8331, Section 28.17.5
ADC Result Registers
• For all result registers and with any ADC result resolution, a signed number is represented in 2's complement form, and the MSB represents the sign bit
• The RESL and RESH register pair represents the 16-bit value, ADCRESULT
> The low byte of the 16-bit register must be read before the high byte
> When the low byte register is read by the CPU, the high byte of the 16-bit register is copied into the temporary register in the same clock cycle as the low byte is read
> When the high byte is read, it is then read from the temporary register
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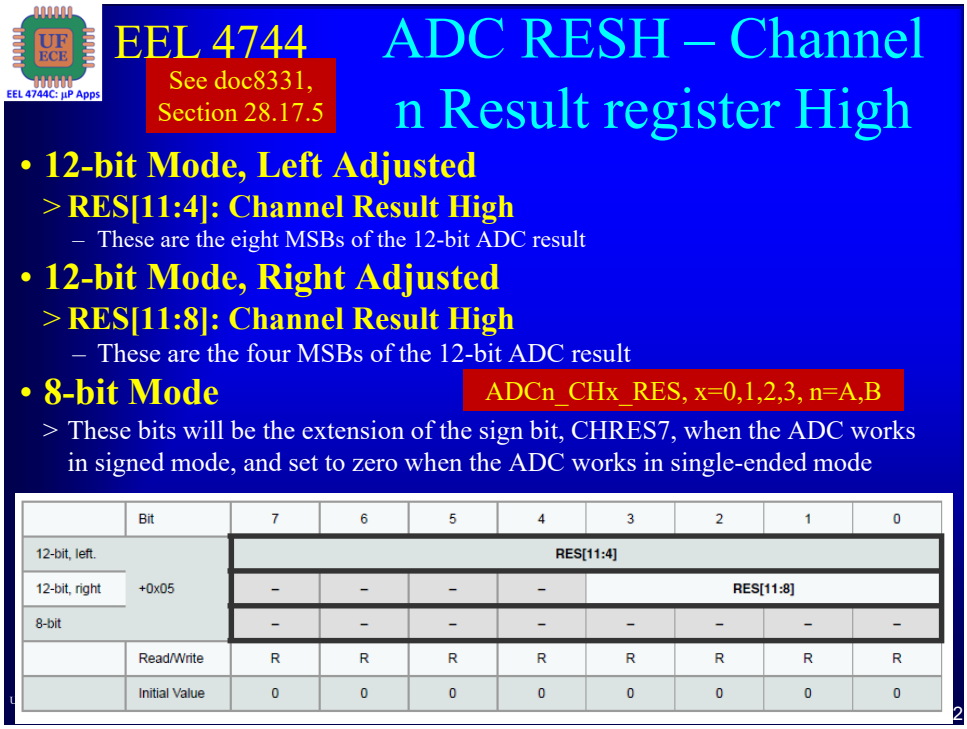
EEL 4744
See doc8331, Section 28.17.5
ADC RESH – Channel n Result register High
• 12-bit Mode, Left Adjusted
> RES[11:4]: Channel Result High
– These are the eight MSBs of the 12-bit ADC result
• 12-bit Mode, Right Adjusted
> RES[11:8]: Channel Result High
– These are the four MSBs of the 12-bit ADC result
• 8-bit Mode
ADCn_CHx_RES, x=0,1,2,3, n=A,B
> These bits will be the extension of the sign bit, CHRES7, when the ADC works in signed mode, and set to zero when the ADC works in single-ended mode
Bit 7 6 5 4 3 2 1 0
12-bit, left. +0x05 RES[11:4]
12-bit, right – – – – RES[11:8]
8-bit – – – – – – – –
Read/Write R R R R R R R R
Initial Value 0 0 0 0 0 0 0 0

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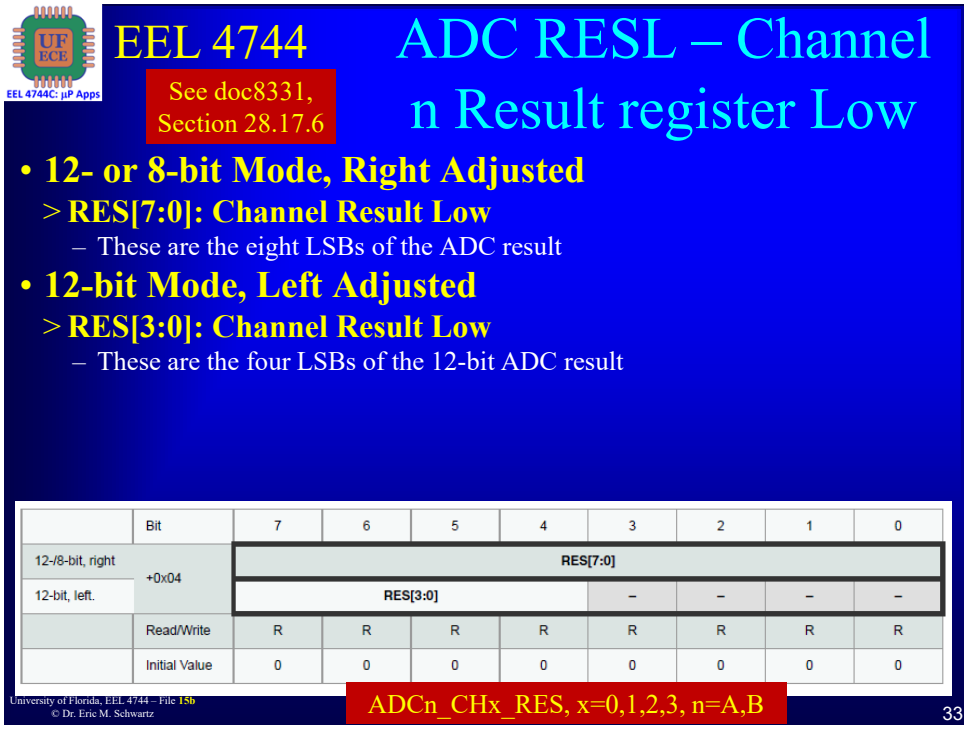
EEL 4744
See doc8331, Section 28.17.6
ADC RESL – Channel n Result register Low
• 12- or 8-bit Mode, Right Adjusted
> RES[7:0]: Channel Result Low
– These are the eight LSBs of the ADC result
• 12-bit Mode, Left Adjusted
> RES[3:0]: Channel Result Low
– These are the four LSBs of the 12-bit ADC result
Bit 7 6 5 4 3 2 1 0
12-/8-bit, right
+0x04
RES[7:0]
12-bit, left.
RES[3:0] – – – –
Read/Write R R R R R R R R
Initial Value 0 0 0 0 0 0 0 0
ADCn_CHx_RES, x=0,1,2,3, n=A,B
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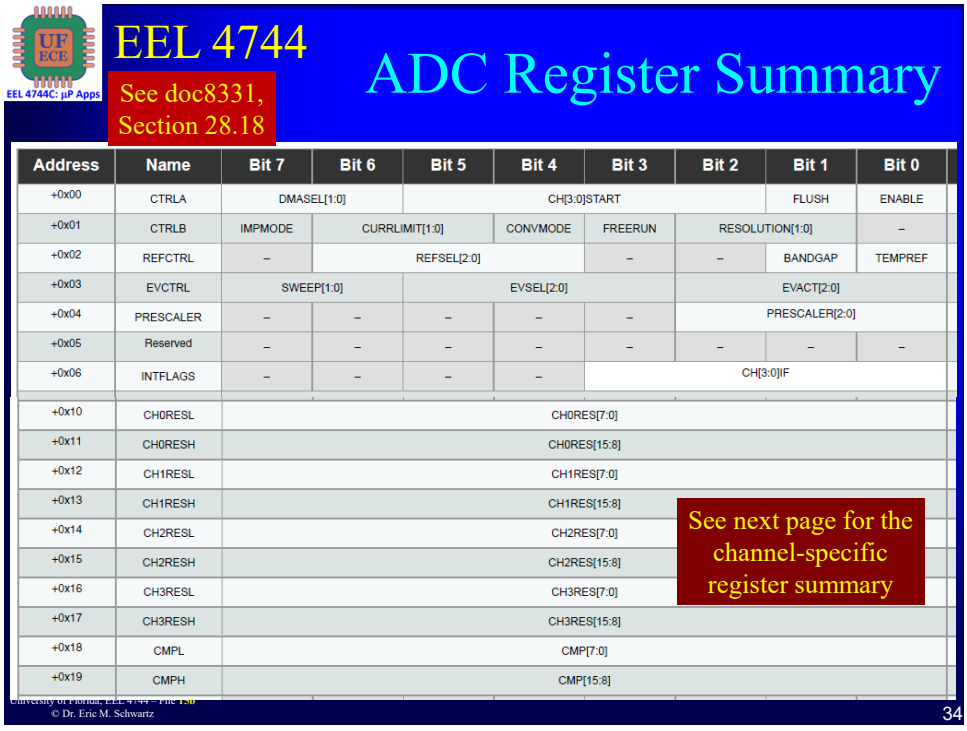
EEL 4744
See doc8331, Section 28.18
ADC Register Summary
Address Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0
+0x00 CTRLA DMASEL[1:0] CH[3:0]START FLUSH ENABLE
+0x01 CTRLB IMPMODE CURRLIMIT[1:0] CONVMODE FREERUN RESOLUTION[1:0] –
+0x02 REFCTRL – REFSEL[2:0] – – BANDGAP TEMPREF
+0x03 EVCTRL SWEEP[1:0] EVSEL[2:0] EVACT[2:0]
+0x04 PRESCALER – – – – – PRESCALER[2:0]
+0x05 Reserved – – – – – – – –
+0x06 INTFLAGS – – – – CH[3:0]IF
+0x10 CH0RESL CH0RES[7:0]
+0x11 CH0RESH CH0RES[15:8]
+0x12 CH1RESL CH1RES[7:0]
+0x13 CH1RESH CH1RES[15:8]
+0x14 CH2RESL CH2RES[7:0]
+0x15 CH2RESH CH2RES[15:8]
+0x16 CH3RESL CH3RES[7:0]
+0x17 CH3RESH CH3RES[15:8]
+0x18 CMPL CMP[7:0]
+0x19 CMPH CMP[15:8]
See next page for the channel-specific register summary
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ADC **Channel** Register Summary

See doc8331, Section 28.19

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
+0x00	CTRL	START	–	–	GAIN[2:0]			INPUTMODE[1:0]	
+0x01	MUXCTRL	–	MUXPOS[3:0]				MUXNEG[2:0]		
+0x02	INTCTRL	–	–	–	–	INTMODE[1:0]		INTLVL[1:0]	
+0x03	INTFLAGS	–	–	–	–	–	–	–	IF
+0x04	RESL	RES[7:0]							
+0x05	RESH	RES[15:8]							
+0x06	SCAN	OFFSET				COUNT			
+0x07	Reserved	–	–	–	–	–	–	–	–

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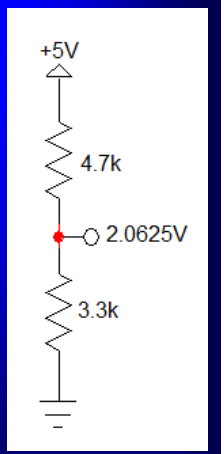
uTinkerer ADC

See uTinkerer Manual, Page 8

- "The uTinkerer, in an effort to reduce external circuitry size and complexity, has built in pre-amplifiers on ADC (port A) inputs **AD0-7**. The pre-amplifiers essentially **remap the range of the XMEGA's ADC from 0 to 2.0625V to** a more flexible **0 to 5V**. The pre-amplifiers are designed to work with the internal ADC voltage reference (VREF) of **VCC/1.6V** (2.0625V when VCC=3.3V)."
- "It should be noted that even though the pre-amplifier circuit increases functionality, it also is another source for analog conversion error. For details, consult the included sensitivity analysis of the analog pre-amplifiers."
- If put 5V on top, get 2.0625V at center tap.



$$VREF = \frac{VCC}{1.6} = \frac{3.3}{1.6} = 2.0625\ \text{V} \qquad \frac{5\ \text{V} * 3.3\text{k}}{4.7\text{k} + 3.3\text{k}} = 2.0625\ \text{V}$$

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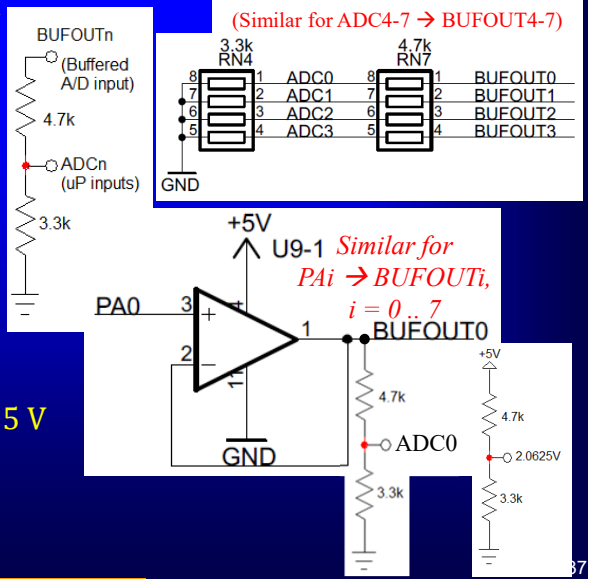
uTinkerer ADC

See uTinkerer Schematics, Sheet 2

- PA0-PA7 are the **external uTinkerer ADC inputs**
  - > Pins are buffered with circuit (on bottom right)
  - > Signals are attenuated with the resistor divider circuit →
  - > PAx pins are on J21
    - – Each PAx can be 0 to 5V
- **ADC0-7 (ADCn) go to the XMEGA ADC pins on ports A**

$$VREF = \frac{VCC}{1.6} = \frac{3.3}{1.6} = 2.0625\ \text{V}$$

$$\frac{5\ \text{V} * 33\text{k}}{47\text{k} + 33\text{k}} = 2.0625\ \text{V}$$



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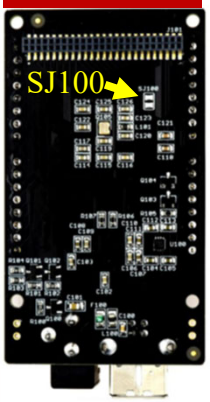
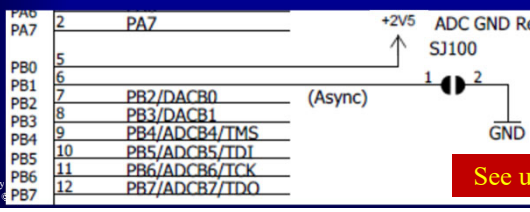
uPAD 2.0 ADC

Back of µPAD 2.0 PCB



- PORTB 0 is the input for the precision 2.5V analog reference
- PORTB 1 is the circuit GND reference input for differential analog measurements
- **If you set the direction register for PORTB pins 0 or 1 to output** (default for all pins is input) **you risk DESTROYING your board!**
  - > **Always use caution when using PORTB of the µPAD's XMEGA!!!**
- The solder jumper SJ100 (on the bottom of the uPAD PCB, highlighted here), connects PB1 to board GND
  - > This GND connection is the negative input for differential measurements and the positive input terminal for differential measurements with gain via the XMEGA's PGA (Programmable Gain Array)



NOT needed our semester

See uPAD 2.0 Schematic

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XMEGA and Sign

- In signed mode, you can interpret negative values, but … you can **NOT** supply voltages lower than the XMEGA's ground.
  - >But consider measuring something with a multimeter at **3.7 V**; now flip the leads and see that it now measures **-3.7 V**.
  - >In differential mode, both voltages must be above the XMEGA's ground, but the differential voltage can be positive or negative.
    - – You will use this for the CdS cell in your Lab 7.
    - – Look at the Analog Backpack schematic (next page) to see both CDS+ and CDS- are above ground (GND).

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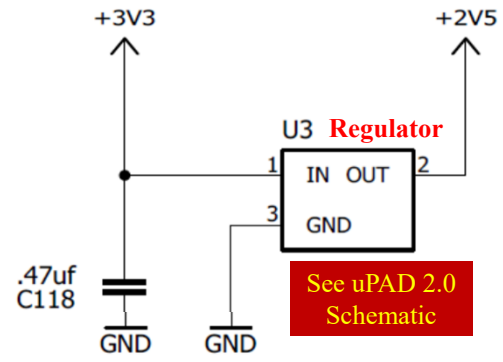
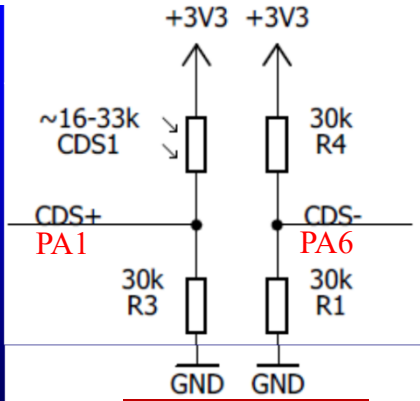
uPAD **2.0** ADC Reference & CdS on Analog Backpack **v1.3**

2.5V Analog Reference



CdS Wheatstone Bridge Circuit (for analog input)



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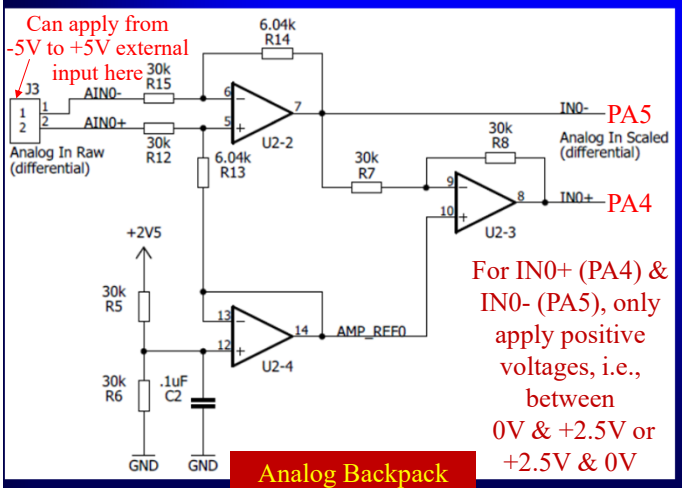
EEL 4744 uPAD Analog Backpack **v1.3**

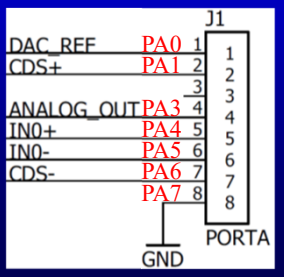
- IN0- and IN0+ are used for differential analog inputs



Analog Backpack v1.3 Schematic

For IN0+ (PA4) & IN0- (PA5), only apply positive voltages, i.e., between 0V & +2.5V or +2.5V & 0V

- If apply a 10V peak-to-peak sine wave at J3, will get a 2V peak-to-peak sine wave centered at 1.25V



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EEL 4744 ADC Register Suggestions For Our Lab

- Enable ADC: **ADCA_CTRLA**
  - The ADC takes up to 24 ADC clocks cycles before it is ready to be used
- Set reference: **ADCA_REFCTRL**
  - > You need to use the value that will make VREF=External AREF pin on PORTB
- Set sample time: **ADCA_PRESCALER**
  - > Al Gore suggests using DIV512
- Set mode (unsigned or signed; single scan or free running) **ADCA_CTRLB**
- Set ADC pin for input: **PORTA_DIR**
- Start the scan: **ADCA_CH0_CTRL**
- Wait for result (or use interrupts): **ADCA_CH0_INTFLAGS**
- Get Result: **ADCA_CH0_RES**
  - > This might be two bytes to deal with, depending on the number of bits and right- or left-adjusted

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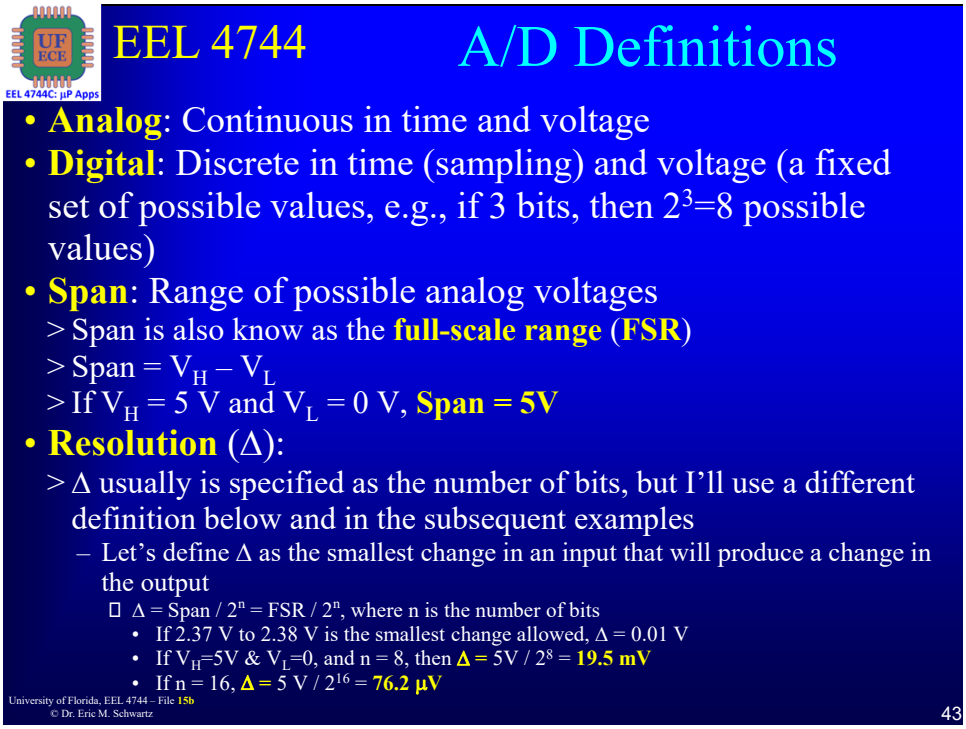
EEL 4744
A/D Definitions
• Analog: Continuous in time and voltage
• Digital: Discrete in time (sampling) and voltage (a fixed set of possible values, e.g., if 3 bits, then 2^3=8 possible values)
• Span: Range of possible analog voltages
> Span is also know as the full-scale range (FSR)
> Span = V_H – V_L
> If V_H = 5 V and V_L = 0 V, Span = 5V
• Resolution (Δ):
> Δ usually is specified as the number of bits, but I'll use a different definition below and in the subsequent examples
– Let's define Δ as the smallest change in an input that will produce a change in the output
Δ = Span / 2^n = FSR / 2^n, where n is the number of bits
• If 2.37 V to 2.38 V is the smallest change allowed, Δ = 0.01 V
• If V_H=5V & V_L=0, and n = 8, then Δ = 5V / 2^8 = 19.5 mV
• If n = 16, Δ = 5 V / 2^16 = 76.2 μV
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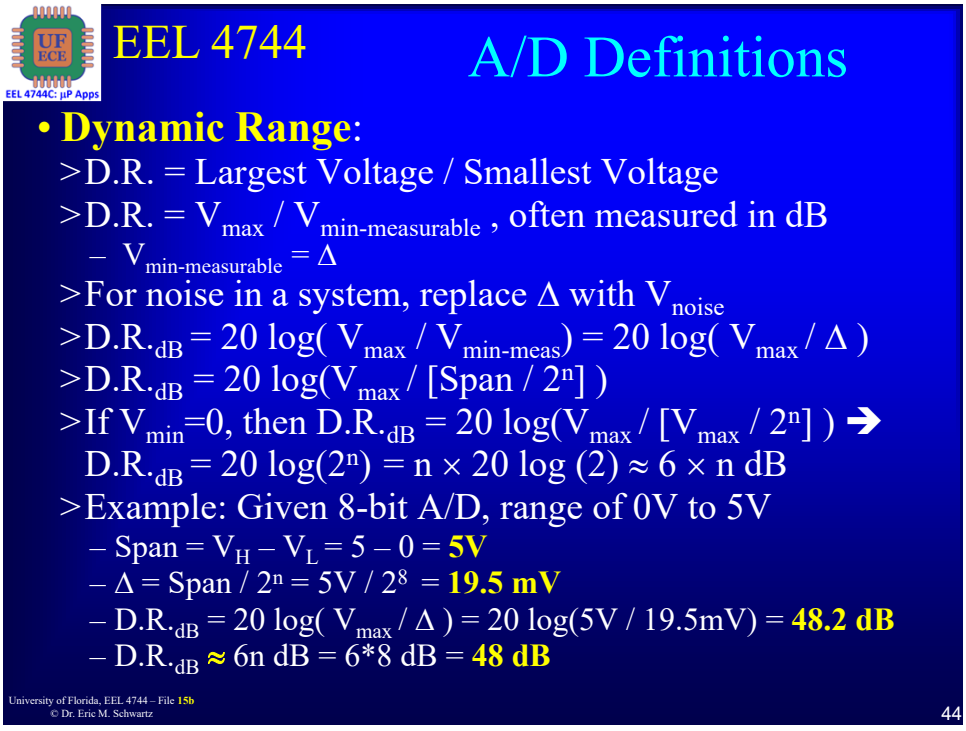
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A/D Definitions
• Dynamic Range:
>D.R. = Largest Voltage / Smallest Voltage
>D.R. = V_max / V_min-measurable , often measured in dB
– V_min-measurable = Δ
>For noise in a system, replace Δ with V_noise
>D.R._dB = 20 log(V_max / V_min-meas) = 20 log(V_max / Δ)
>D.R._dB = 20 log(V_max / [Span / 2^n])
>If V_min=0, then D.R._dB = 20 log(V_max / [V_max / 2^n]) ➔
D.R._dB = 20 log(2^n) = n × 20 log (2) ≈ 6 × n dB
>Example: Given 8-bit A/D, range of 0V to 5V
– Span = V_H – V_L = 5 – 0 = 5V
– Δ = Span / 2^n = 5V / 2^8 = 19.5 mV
– D.R._dB = 20 log(V_max / Δ) = 20 log(5V / 19.5mV) = 48.2 dB
– D.R._dB ≈ 6n dB = 6*8 dB = 48 dB
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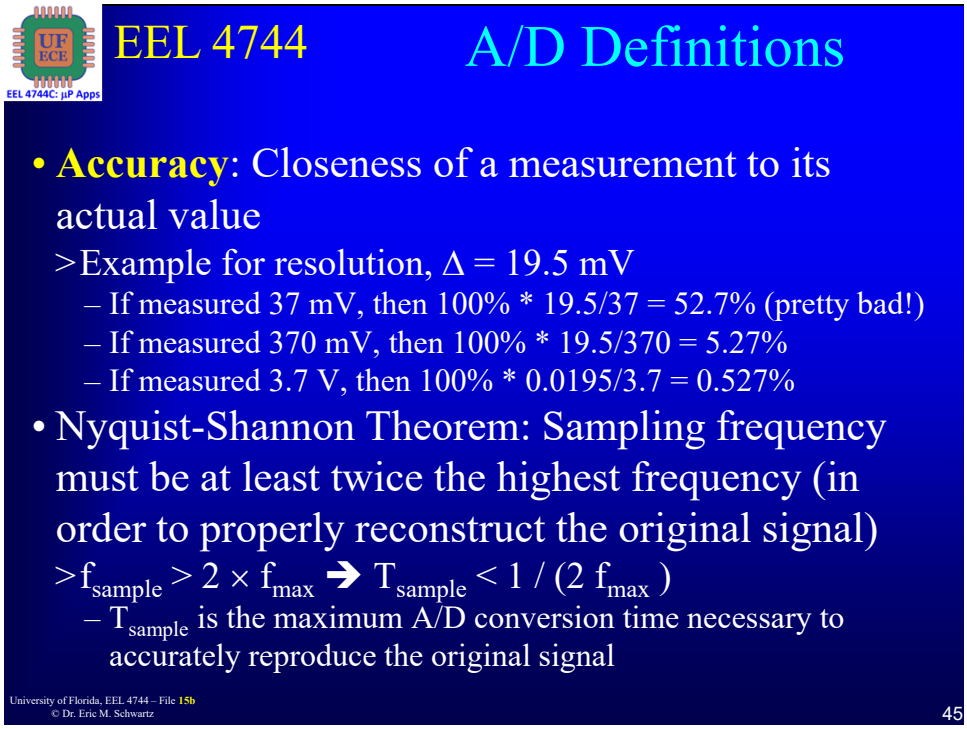
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A/D Definitions
• Accuracy: Closeness of a measurement to its actual value
>Example for resolution, Δ = 19.5 mV
– If measured 37 mV, then 100% * 19.5/37 = 52.7% (pretty bad!)
– If measured 370 mV, then 100% * 19.5/370 = 5.27%
– If measured 3.7 V, then 100% * 0.0195/3.7 = 0.527%
• Nyquist-Shannon Theorem: Sampling frequency must be at least twice the highest frequency (in order to properly reconstruct the original signal)
>$f_{sample} > 2 \times f_{max}$ ➔ $T_{sample} < 1 / (2 f_{max})$
– T_{sample} is the maximum A/D conversion time necessary to accurately reproduce the original signal
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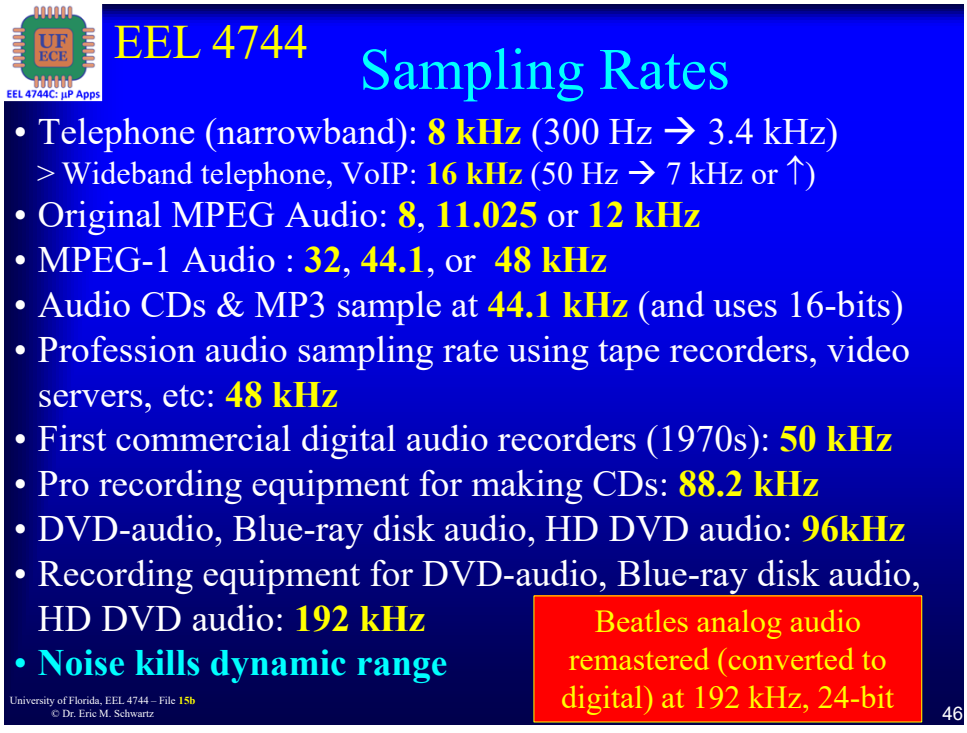
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Sampling Rates
• Telephone (narrowband): 8 kHz (300 Hz ➔ 3.4 kHz)
> Wideband telephone, VoIP: 16 kHz (50 Hz ➔ 7 kHz or ↑)
• Original MPEG Audio: 8, 11.025 or 12 kHz
• MPEG-1 Audio : 32, 44.1, or 48 kHz
• Audio CDs & MP3 sample at 44.1 kHz (and uses 16-bits)
• Profession audio sampling rate using tape recorders, video servers, etc: 48 kHz
• First commercial digital audio recorders (1970s): 50 kHz
• Pro recording equipment for making CDs: 88.2 kHz
• DVD-audio, Blue-ray disk audio, HD DVD audio: 96kHz
• Recording equipment for DVD-audio, Blue-ray disk audio, HD DVD audio: 192 kHz
• Noise kills dynamic range
Beatles analog audio remastered (converted to digital) at 192 kHz, 24-bit
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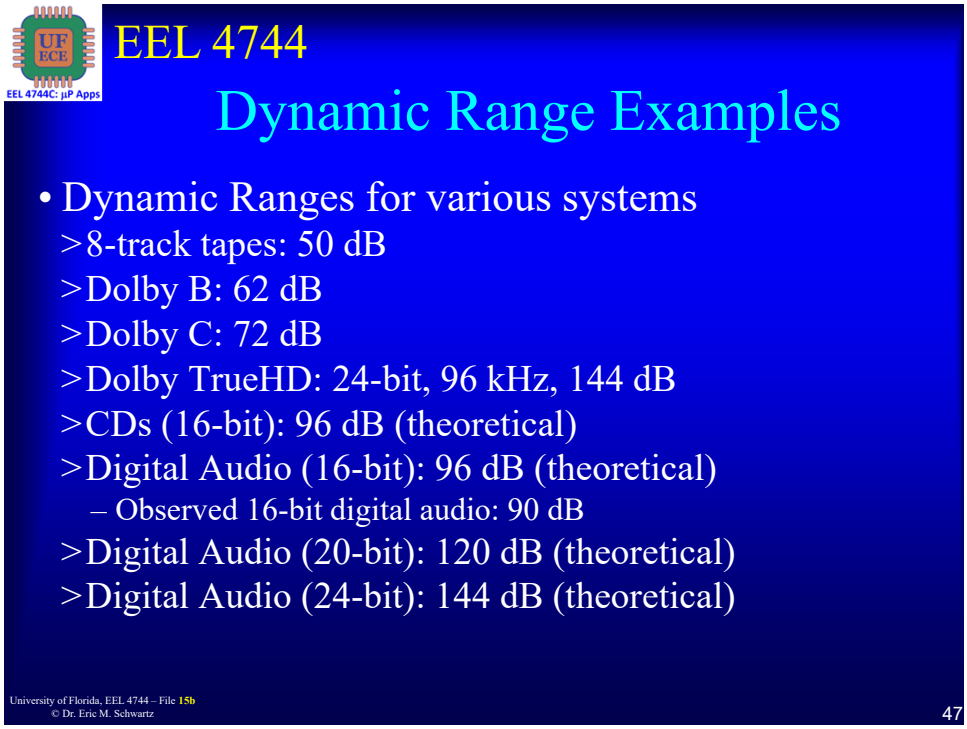
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Dynamic Range Examples
• Dynamic Ranges for various systems
>8-track tapes: 50 dB
>Dolby B: 62 dB
>Dolby C: 72 dB
>Dolby TrueHD: 24-bit, 96 kHz, 144 dB
>CDs (16-bit): 96 dB (theoretical)
>Digital Audio (16-bit): 96 dB (theoretical)
– Observed 16-bit digital audio: 90 dB
>Digital Audio (20-bit): 120 dB (theoretical)
>Digital Audio (24-bit): 144 dB (theoretical)
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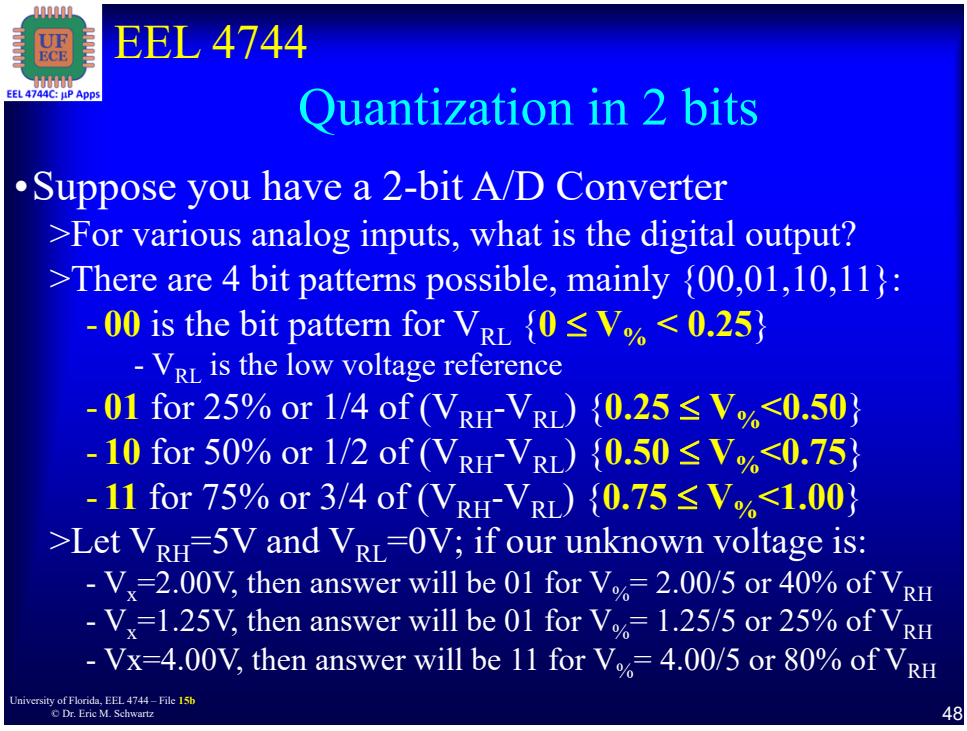
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Quantization in 2 bits
•Suppose you have a 2-bit A/D Converter
>For various analog inputs, what is the digital output?
>There are 4 bit patterns possible, mainly {00,01,10,11}:
- 00 is the bit pattern for V_{RL} {0 ≤ $V_{\%}$ < 0.25}
- V_{RL} is the low voltage reference
- 01 for 25% or 1/4 of (V_{RH}-V_{RL}) {0.25 ≤ $V_{\%}$<0.50}
- 10 for 50% or 1/2 of (V_{RH}-V_{RL}) {0.50 ≤ $V_{\%}$<0.75}
- 11 for 75% or 3/4 of (V_{RH}-V_{RL}) {0.75 ≤ $V_{\%}$<1.00}
>Let V_{RH}=5V and V_{RL}=0V; if our unknown voltage is:
- V_x=2.00V, then answer will be 01 for $V_{\%}$= 2.00/5 or 40% of V_{RH}
- V_x=1.25V, then answer will be 01 for $V_{\%}$= 1.25/5 or 25% of V_{RH}
- Vx=4.00V, then answer will be 11 for $V_{\%}$= 4.00/5 or 80% of V_{RH}
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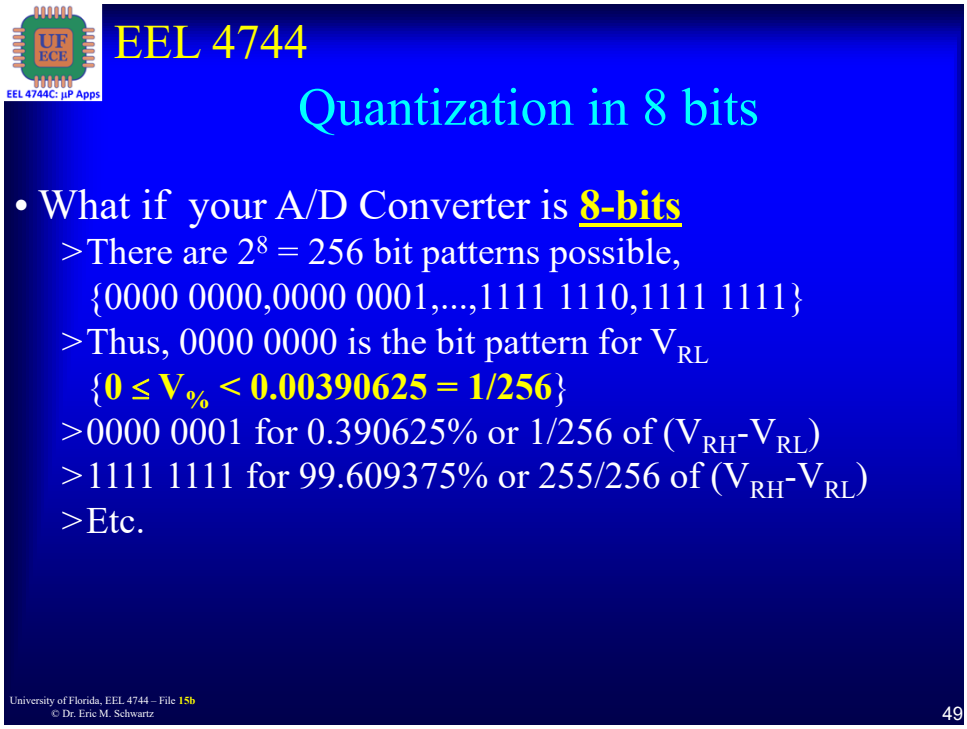
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Quantization in 8 bits
• What if your A/D Converter is 8-bits
>There are 2^8 = 256 bit patterns possible,
{0000 0000,0000 0001,...,1111 1110,1111 1111}
>Thus, 0000 0000 is the bit pattern for V_{RL}
{0 ≤ $V_{\%}$ < 0.00390625 = 1/256}
>0000 0001 for 0.390625% or 1/256 of (V_{RH}-V_{RL})
>1111 1111 for 99.609375% or 255/256 of (V_{RH}-V_{RL})
>Etc.
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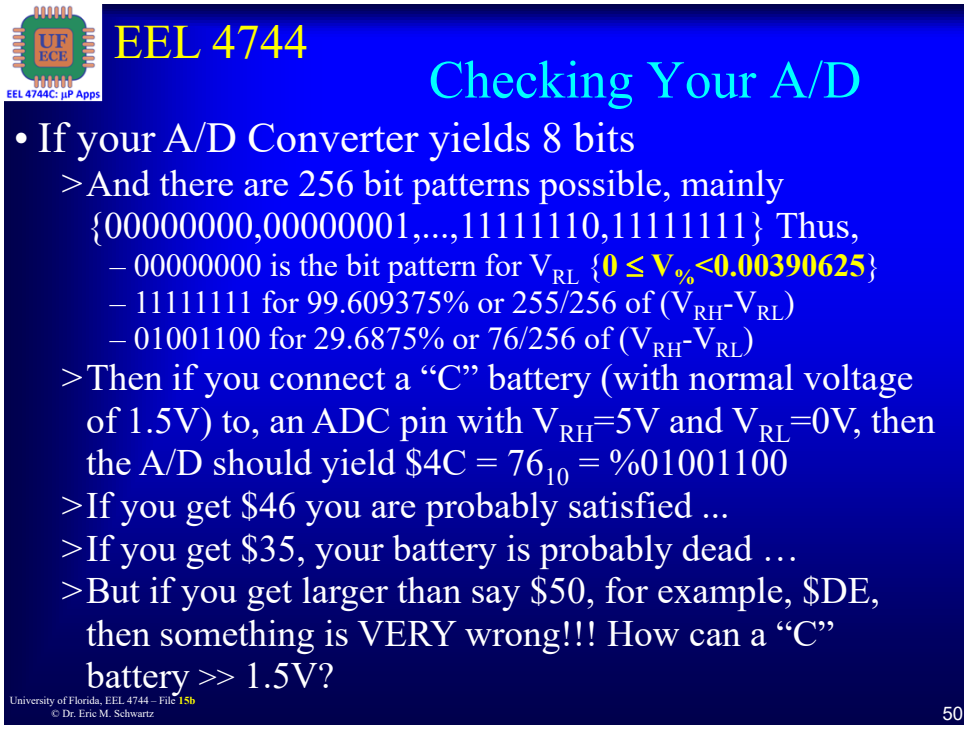
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Checking Your A/D
• If your A/D Converter yields 8 bits
>And there are 256 bit patterns possible, mainly
{00000000,00000001,...,11111110,11111111} Thus,
– 00000000 is the bit pattern for V_{RL} {0 ≤ $V_{\%}$<0.00390625}
– 11111111 for 99.609375% or 255/256 of (V_{RH}-V_{RL})
– 01001100 for 29.6875% or 76/256 of (V_{RH}-V_{RL})
>Then if you connect a "C" battery (with normal voltage of 1.5V) to, an ADC pin with V_{RH}=5V and V_{RL}=0V, then the A/D should yield $4C = 76_{10} = %01001100
>If you get $46 you are probably satisfied ...
>If you get $35, your battery is probably dead …
>But if you get larger than say $50, for example, $DE, then something is VERY wrong!!! How can a "C" battery >> 1.5V?
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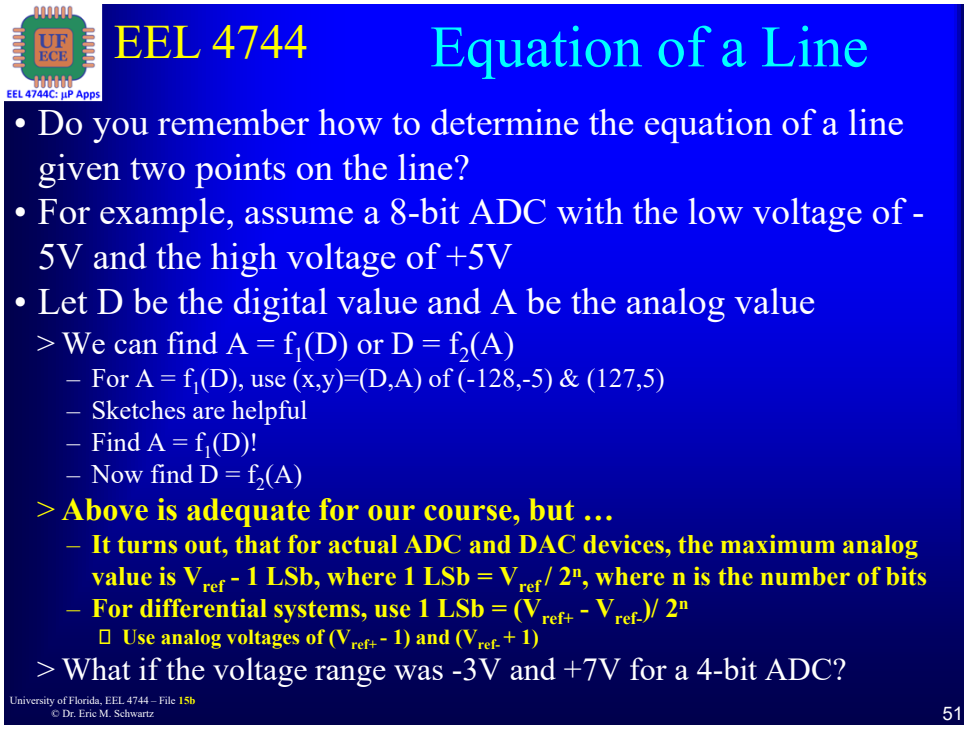
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Equation of a Line
• Do you remember how to determine the equation of a line given two points on the line?
• For example, assume a 8-bit ADC with the low voltage of -5V and the high voltage of +5V
• Let D be the digital value and A be the analog value
> We can find A = f1(D) or D = f2(A)
– For A = f1(D), use (x,y)=(D,A) of (-128,-5) & (127,5)
– Sketches are helpful
– Find A = f1(D)!
– Now find D = f2(A)
> Above is adequate for our course, but …
– It turns out, that for actual ADC and DAC devices, the maximum analog value is Vref - 1 LSb, where 1 LSb = Vref / 2n, where n is the number of bits
– For differential systems, use 1 LSb = (Vref+ - Vref-)/ 2n
Use analog voltages of (Vref+ - 1) and (Vref- + 1)
> What if the voltage range was -3V and +7V for a 4-bit ADC?
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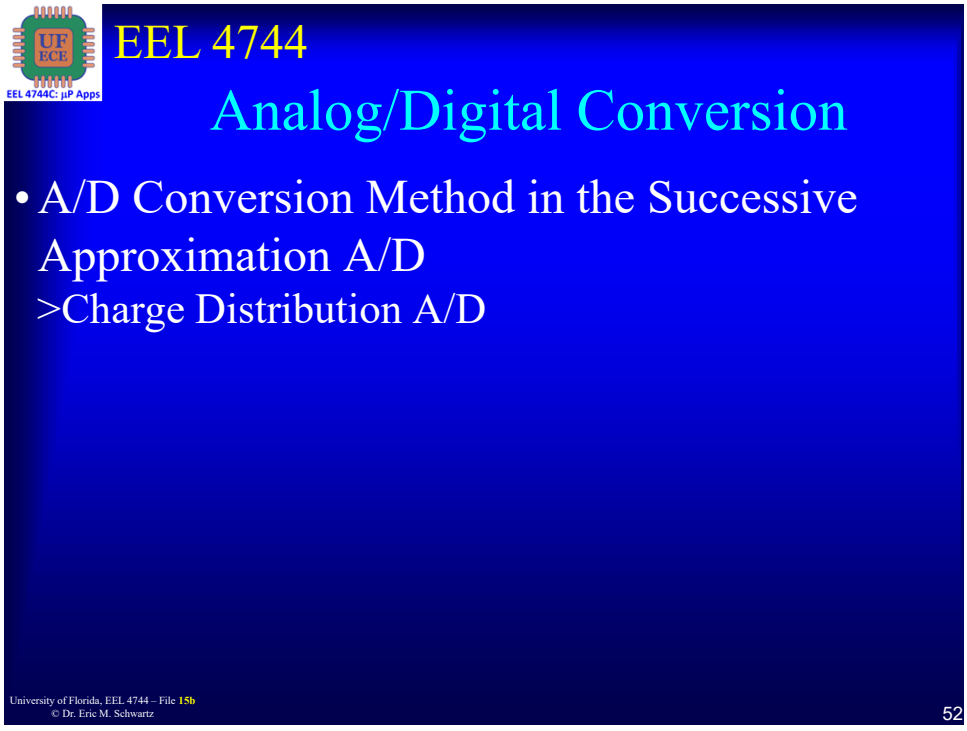
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Analog/Digital Conversion
• A/D Conversion Method in the Successive Approximation A/D
>Charge Distribution A/D
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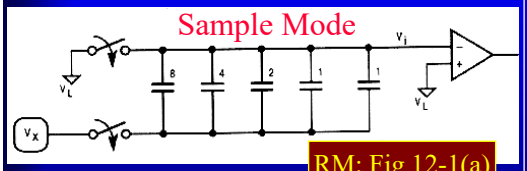
Basic Charge-Redistribution A/D

a) Sample Mode

the Total Charge: $Q_S = C\,V$

$Q_S = 16\,(V_X - V_L)$

$\therefore Q_S = 16\,V_X$ (with $V_L = 0$)

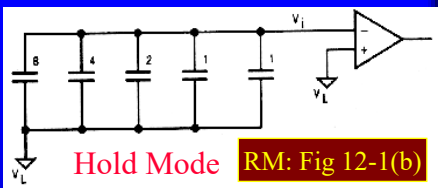


RM: Fig 12-1(a)

b) Hold Mode (see figure, next column)

$Q_H = (V_L - V_i)\,16$

$\therefore Q_H = -16\,V_i$ (with $V_L = 0$)



RM: Fig 12-1(b)

Since charge is conserved,

$Q_S = Q_H$

$16\,V_X = -16V_i$

$V_X = -V_i$

$\therefore V_i = -V_X$

c) Approximation Mode

RM: Fig 12-1(c)

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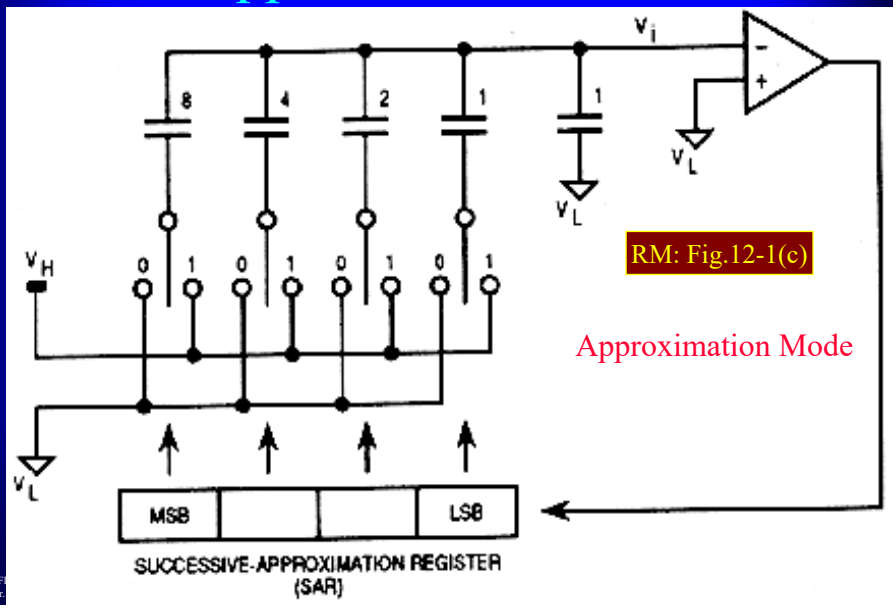
Approximation Mode



RM: Fig.12-1(c)

Approximation Mode

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A Conversion Sequence Example (4 bit)

Let $V_X = 21/32\ V_H$

During the sample time,

$Q_S = 16\ V_X = (16)\ 21/32\ V_H$

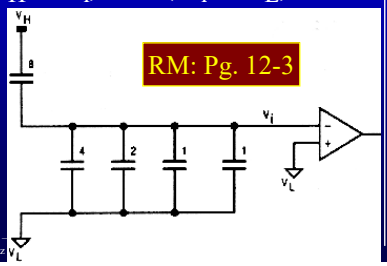
$\therefore$ **$Q_S = 21/2\ V_H$**

During hold,

$\therefore\ V_i = -V_X = -21/32\ V_H$

• 8-unit capacitor: $V_L \rightarrow V_H$

$Q = 8\ (V_H - V_i) - 8\ (V_i - V_L)$



with $V_L = 0 \Rightarrow$

$Q = 8V_H - 16\ V_i$

By charge conservation, this charge is set equal to the original charge ($Q_S = Q$):

$21/2\ V_H = 8V_H - 16\ V_i$

Solving for V_i,

$16\ V_i = 8V_H - 21/32\ V_H$

$\therefore V_i = -5/32\ V_H$

(when $V_i<0$, comparator output = 1; when $V_i>0$, comparator output = 0)

$\therefore$ the output of comparator = 1

$\Rightarrow 1???_2$ (and leave 8-unit cap at V_H)

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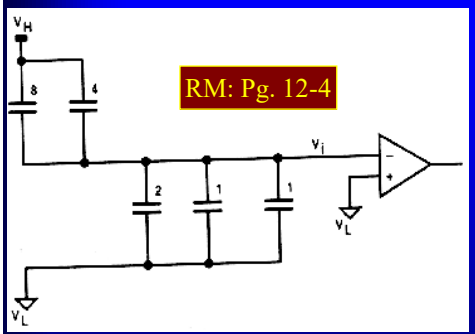
A Conversion Sequence Example (4 bit)

> 4-unit capacitor: $V_L \rightarrow V_H$



$Q = 12\ (V_H - V_i) - 4\ (V_i - V_L)$

with $V_L = 0 \Rightarrow$

$Q = 12V_H - 16\ V_i$

By charge conservation,

$21/2\ V_H = 12V_H - 16\ V_i$

Solving for V_i,

$\therefore V_i = +3/32\ V_H$

(when $V_i<0$, comparator output = 1; when $V_i>0$, comparator output = 0)

$\therefore$ the output of comparator = 0

$\Rightarrow 10??_2$ (and reconnect 4-unit cap to V_L)

$\therefore$ Digital result of this example ($21/32\ V_H$) conversion $\Rightarrow 10??_2$

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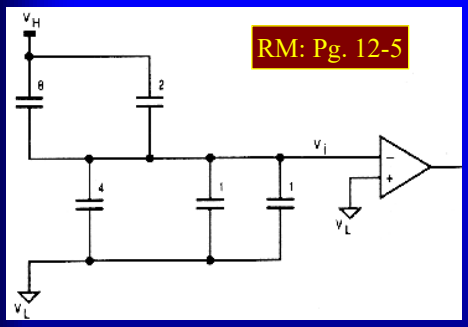
A Conversion Sequence Example (4 bit)

> 2-unit capacitor: $V_L \rightarrow V_H$



$Q = 10\,(V_H - V_i) - 6\,(V_i - V_L)$

with $V_L = 0 \Rightarrow$

$Q = 10V_H - 16\,V_i$

By charge conservation,

$21/2\,V_H = 10V_H - 16\,V_i$

Solving for V_i,

$\therefore V_i = -1/32\,V_H$

(when $V_i<0$, comparator output = 1; when $V_i>0$, comparator output = 0)

$\therefore$ the output of comparator = 1

$\Rightarrow 101?_2$ (and leave 2-unit cap at V_H)

$\therefore$ Digital result of this example ($21/32\,V_H$) conversion $\Rightarrow$ **101**$?_2$

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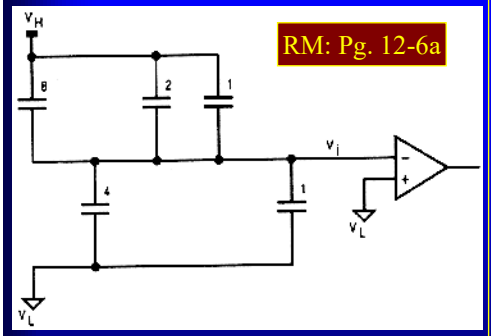
A Conversion Sequence Example (4 bit)

> 1-unit capacitor: $V_L \rightarrow V_H$



$Q = 11\,(V_H - V_i) - 5\,(V_i - V_L)$

with $V_L = 0 \Rightarrow$

$Q = 11V_H - 16\,V_i$

By charge conservation,

$21/2\,V_H = 11V_H - 16\,V_i$

Solving for V_i,

$V_i = +1/32\,V_H$

(when $V_i<0$, comparator output = 1; when $V_i>0$, comparator output = 0)

$\therefore$ the output of comparator = 0

$\Rightarrow 1010_2$ (done!)

$\therefore$ Digital result of this example ($21/32\,V_H$) conversion $\Rightarrow$ **1010**$_2$ ($10/16\,V_H$)

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EEL 4744C: µP Apps
The End!
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